100V, 0.8A Step-down Converter

DESCRIPTION

The CS5525E is a high efficiency asynchronous step-down converter with integrated high-side and low-side MOSFETs. It provides 0.8A output in buck topology from up to 100V input power supply.

The CS5525E adopts constant-on-time (COT) control mode that provides fast transient response and facilitates loop stabilization. Operation frequency can be programmed easily from 100kHz to 1MHz by an external resistor.CS5525E supports high efficiency pulse-skipmode (PSM) in light load condition. Valley current limit circuits protect against overload and short circuit conditions.

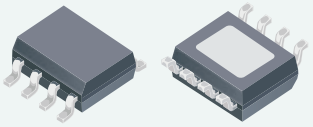
The CS5525E is available in a ESOP8 packages.

FEATURES

- 10V-to-100V Input Voltage Range
- 1V-to-30V Output Voltage Range
- 90% Maximum Operation Duty Cycle
- 625mΩ / 380mΩ Internal MSOFETs
- Constant On Time Control Mode
- Programmable 100kHz to 1MHz Frequency
- Internal Soft-Start and Loop Compensation
- OCP, SCP with Hiccup
- High Efficiency PSM in Light Load
- Available in ESOP8 Package

Package

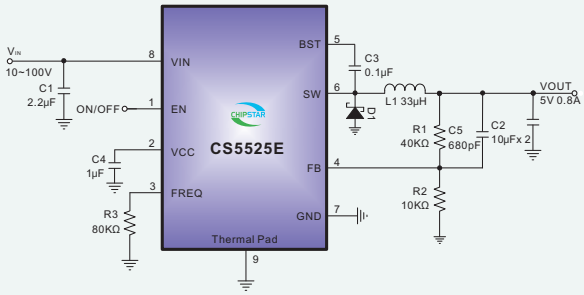
- ESOP8

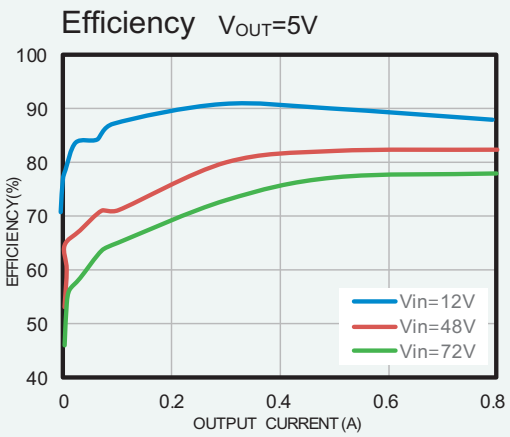


APPLICATIONS

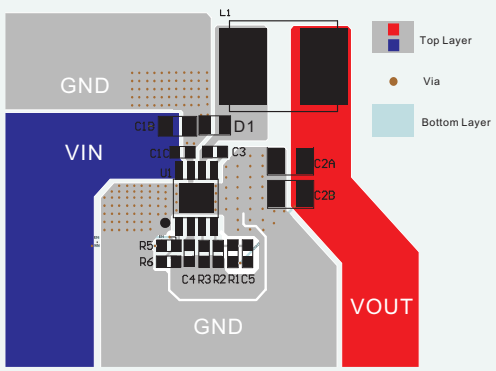
- E-bike GPS Tracker
- Industrial Power Supplies
- Printer Power Board

TYPICAL APPLICATION CIRCUIT

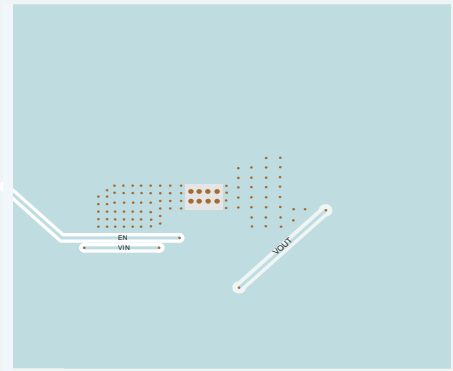




Sample Board Layout

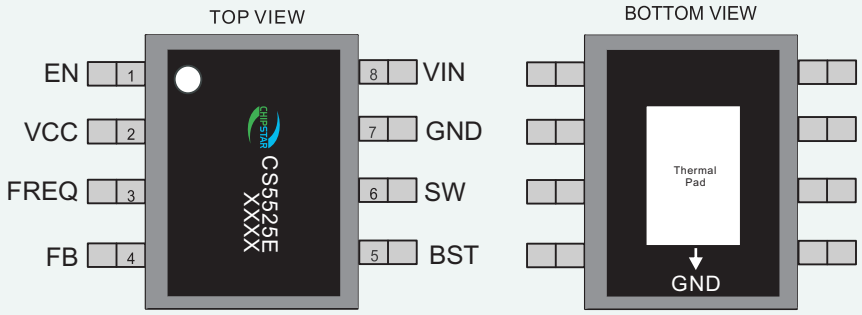


Top Layer



Bottom Layer

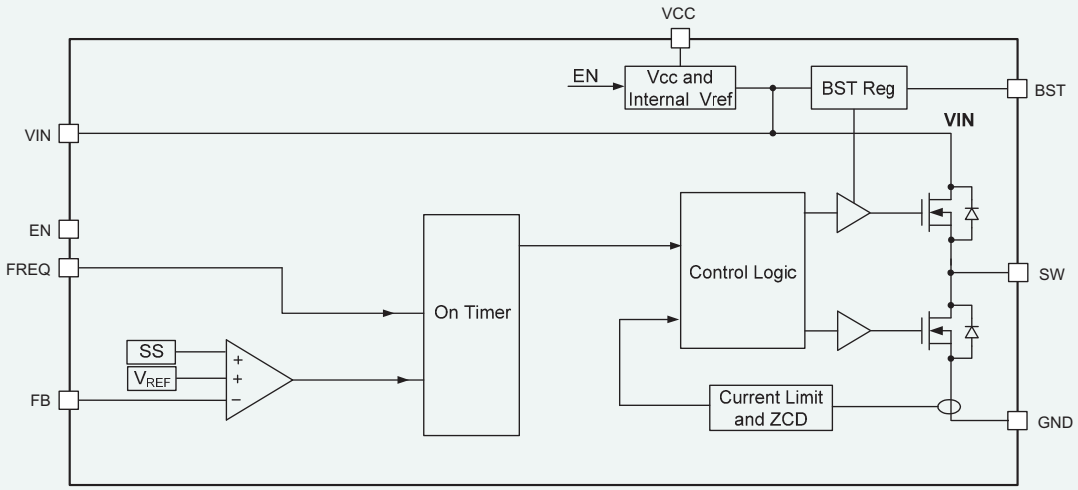
PIN CONFIGURATION (ESOP8L)



PIN FUNCTIONS

Pin #	Name	Description
1	EN	Power enable pin. Pull high to enable CS5525E, pull low to disable MP4581. It cannot float, must be pulled high to enable the IC or pulled low to disable the IC.
2	VCC	**Internal LDO output**. Supply power to internal control circuit. Decoupling with≥1μF ceramic capacitor.
3	FREQ	**Switching frequency set pin**. An external resistor from this pin to GND sets the buck switching frequency.
4	FB	**VOUT voltage feedback pin**. Connect a resistor divider from VOUT to FB.
5	BST	**Bootstrap power pin for high-side MOSFET Gate Driver**. Connect one 0.1μF capacitor between BST and SW.
6	SW	**Switch node of the converter**. Connect to the source of the high-side FET and drain of the low-side FET.
7	GND	**Power ground pin**.
8	VIN	**Power supply input pin**.
9	GND	**Thermal pad**

FUNCTION DIAGRAM



Functional Block Diagram

Absolute Maximum Ratings [1]

Symbol	Description	Value	Unit
VIN,EN,SW		0.3 to 105	V
BST to SW		-0.3 to 6	V
All other PIN		-0.3 to 6	V
T_J	Operating Junction Temperature Range	-40 to 150	℃
T_{SDR}	Maximum Lead Soldering Temperature , 10 Seconds	260	℃
T_{STG}	Storage Temperature Range	-65 to 150	℃

Recommended Operating Conditions

Symbol	Description	Value	Unit
VIN	Supply Voltage	10~100	V
VOUT	Output Voltage	1~30	v
T_j	Junction Temperature Range	-40~125	℃

Thermal Information [2]

Symbol	Description	Value	Unit
θ_{JA}(ESOP8)	Thermal Resistance-Junction to Ambient	40	°C/W
θ_{JC}(ESOP8)	Thermal Resistance-Junction to Case	15	°C/W

Ordering and Marking Information

Device	Package Type	Device Marking	Quantity
CS8511E	ESOP-8L		IC TUBE (100 units)

ESD Susceptibility

ESD Susceptibility- H B M ---------- ±2kV
ESD Susceptibility- M M ----------±200V

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent dmage to thedevice.Functional operation at conditions other than the operating conditions specified is not implied.Only one Absolute Maximum Rating should be applied at one time.
2. The Thermal Pad on the bottom of the IC should soldered directly to the PCB's Thermal Pad area that with several thermal vias connect to the ground plan,and the PCB is a 2-layer,5-inch square area with 2oz copper thickness.

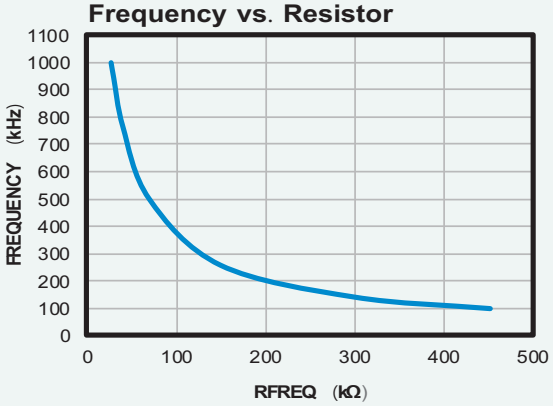
ELECTRICAL CHARACTERISTICS V_{IN} = 48V, T_J= 25℃, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
VCC Under Voltage Lockout Threshold Rising	VCC_{UVLO-R}	VCC Rising	3.45	3.9	4.35	V
VCC Under Voltage Lockout Threshold Hysteresis	VCC_{HYS}			650		mV
VCC Regulation Voltage		I_{VCC}=2mA	4.5	4.85	5.2	V
Shutdown Current	I_{SD}	V_{EN} = 0V, Measured on VIN pin		1		μA
Quiescent Current	I_Q	V_{IN}=12V, V_{FB} =1.05V, no switching, measured on VIN pin		15		μA
Enable Control						
Micro Power EN Startup Threshold					0.9	V
Micro Power EN Off Threshold			0.4			V
EN Input High Threshold	V_{EN-ON}	V_{EN} Rising	1.15	1.25	1.35	V
EN Hysteresis	V_{EN-H}	V_{EN} Rising/Falling		90		mV
Frequency						
Minimum Off Time	$t_{MIN-OFF}$ V	$_{FB}$ = 0V		150		ns
Minimum On Time(6) t	$_{MIN-ON}$			45		ns
Reference Voltage						
FB Reference Voltage	V_{REF}	10V to 100V, T_J = 25℃	0.99	1	1.01	V
FB Input Current	I_{FB}	V_{FB}=1.05V			50	nA
Soft-Start Time	t_{SS}	10% to 90% of V_{REF}	4.35	ms		
FB Under Voltage Threshold	VUVP			60%		VREF
Power Switch						
Low-Side Switch On-Resistance	R_{ON-L}			380		mΩ
High-Side Synchronous Switch On-Resistance	R_{ON-H}			625		mΩ
Low-Side Switch Leakage Current		EN=0V, V_{SW}=100V			0.1	μA
High-Side Switch Leakage Current		EN=0V, V_{IN}=100V, V_{SW}=0V			0.1	μA
Current Limit						
Low Side Valley Current Limit	$I_{VL-LIMT}$	Over full duty cycle	0.72	0.8	0.88	A
Inductor Current ZCD Threshold			-60	0	60	mA
Thermal Protection						
Thermal Shutdown	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{SD-HYS}			25		℃

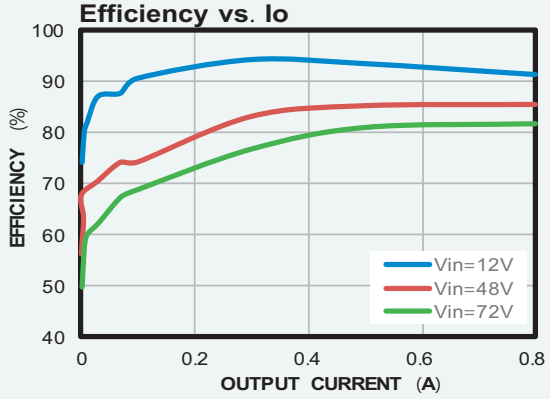
TYPICAL PERFORMANCE CHARACTERISTICS

VIN= 48V, V OUT= 5V, L = 33 µH, TA= 25℃, unless otherwise noted.

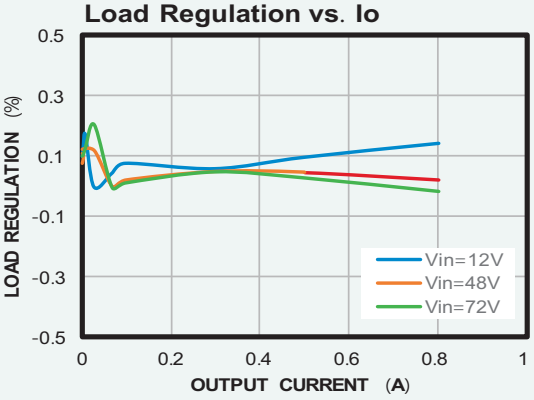
Frequency vs. Resistor



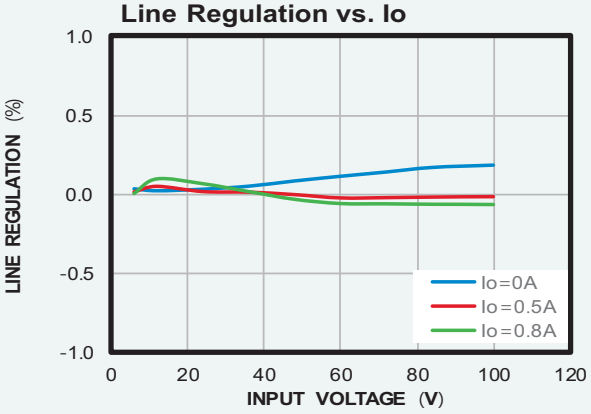
Efficiency vs. Io



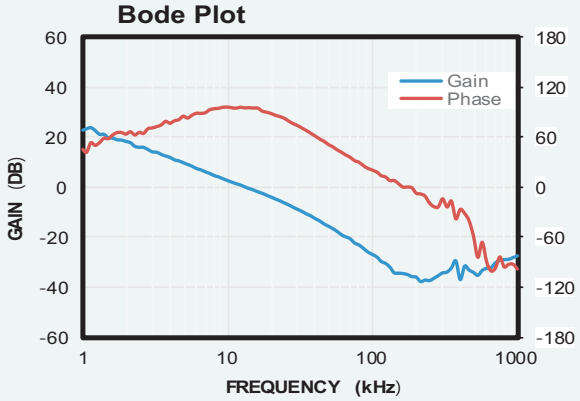
Load Regulation vs. Io



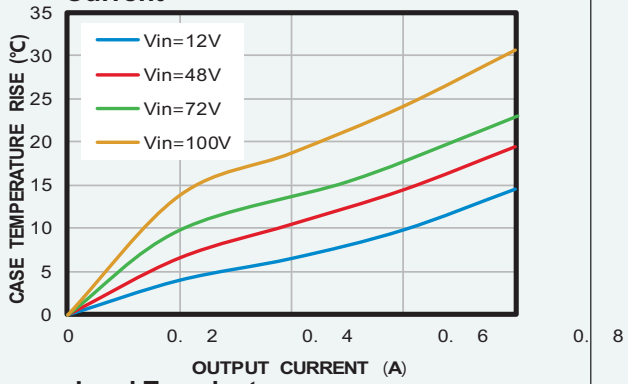
Line Regulation vs. Io



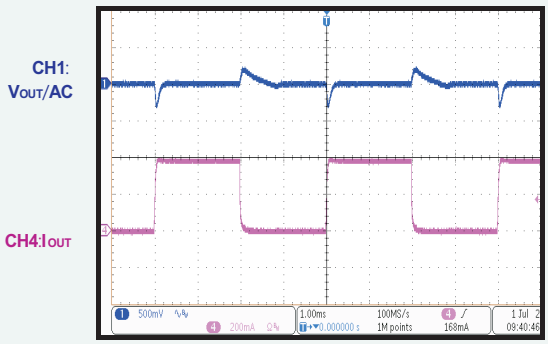
Bode Plot



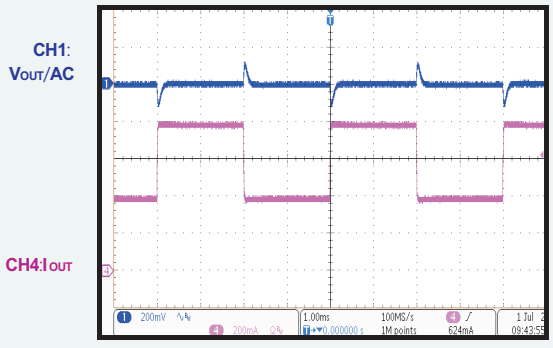
Case Temperature Rise. vs. Output Current



Load Transient I_{OUT}=0A to 0.4A



Load Transient I_{OUT}=0.4A to 0.8A



OPERATION

The CS5525E is a asynchronous, step-down,switching regulator with integrated high-sideand low-side power MOSFETs. It provides a highly-efficient solution with COT control for fast loop response and easy loop stabilization. It features a wide input voltage range, internal soft-start control, and precise current limiting. The very low operational quiescent current makes it suitable for light load high efficiency application.

COT Operation

CS5525E works with Constant-on-time (COT) control mode. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON for a fixed on time when the FB voltage drops below reference voltage. The fixed on time is determined by one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range. After the ON period elapses, the HS-FET is turned off until next period. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There will be a dead short between VIN and GND if both HSFET and LS-FET are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

Heavy-Load Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). In CCM mode, HS-FET is turned on, after the ON period, the HS-FET is turned off, and then low-side MOSFET (LS-FET) is turned on to conduct the inductor current. In CCM mode operation, the switching frequency is fairly constant and it is called PWM mode.

Light-Load Operation

CS5525E can works in PSM in light load. In PSM mode, the LS-FET driver goes into tri-state (high Z) when inductor current drops near zero, the output capacitors discharge slowly to GND through FB feedback resistor. If VOUT drops and internal COMP rises, MP4581 starts the next switching cycle by turning on HS-FET again. CS5525E automatically reduces the switching frequency and reduce the quiescent current when the IC is not switching. This operation greatly improves device efficiency when the output current is low. In light-load PSM operation, the HS-FET does not turn on as frequently as during heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches the critical level when the valley inductor current rises to 0A, and can be determined using the following equation:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}}$$

Where, FSW is the switching frequency.The device reverts to CCM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Power Supply

CS5525E control circuit is powered by VCC,which is regulated from VIN.There is one VCC_UVLO circuit protecting the chipfrom operating at an insufficient supply voltage. The CS5525E UVLO comparator monitors the voltage of VCC and start work when VCC is high enough.

Start Up

When EN is high and VCC is higher than UVLO, CS5525E start up with internal SS signal. After CS5525E starts switching, SS signal ramps up from 0V and compared with the reference voltage, the lower one will feed to the error amplifier to control output voltage. After SS signal rises to above reference voltage, softstart completes and internal reference takes charge of the feedback loop regulation. CS5525E has been designed for monotonic startup into pre-biased loads. If the output is pre-biased to a certain voltage during startup, the voltage on the soft-start capacitor will be charged and if soft-start capacitor voltage exceeds the sensed output voltage at the FB pin, the part starts to work normally.

Enable (EN) and Programmable UVLO

EN pin enables and disables the CS5525E.When applying a voltage higher than 0.9V,CS5525E will start internal BG circuit. After the voltage rise to the EN high threshold (1.25V typically), the CS5525E enables all functions and starts switching operation . Switching operation is disabled when EN voltage falls below its lower threshold (1.16V). EN pin can be compatible with voltage up to 100V. There isn't any internal pull up or pull down resistor on EN pin, tie EN to VIN through a resistor for automatic start up.

Over Load and Short Circuit Protection

CS5525E has valley current limit control. During LS-FET ON state, the inductor current is monitored. When the sensed inductor current is higher the valley current limit,the LS limit

comparator turns over, HS-FET will wait until inductor current falls below valley current limit to turn on again. Meanwhile, the output voltage (VFB) may drop below the under-voltage (UV) threshold—typically 60% of the reference voltage. Once VOUT UV is triggered, the CS5525E enters hiccup mode to periodically restart the part. During soft-start period, the hiccup protection is disabled. During over-current hiccup protection, the chip disables output power stage, discharge softstart cap and then automatically try to soft-start again. If the over-current condition still exists after soft-start ends, the device repeats this hiccup operation till over-current conditions disappear and then output rises back to regulation level.

BST Power Supply

An external bootstrap capacitor powers the floating power MOSFET driver. The external bootstrap capacitor is charged by VCC. And the VBST-VSW voltage can supply the power of HSFET driver. If both VCC and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits. Three events can shut down the chip: EN low, VCC low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The BST floating driver is not subject to this shutdown command.

Thermal Protection

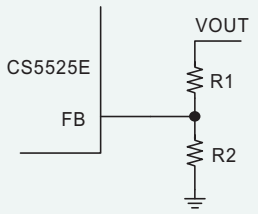
CS5525E integrates one temperature monitor circuit. Once junction temperature is higher than 150°C, CS5525E shuts down. After the temperature drops below 125°C, the power supply resumes operation again.

Setting the Output Voltage

The external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 10kΩ-100kΩ for R2. Then R1 is determined as follow:

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2$$

Where the VREF is the reference voltage, it is 1Vtypically. The feedback circuit is shown as Figure:



PCB Layout Guidelines

Proper layout of the switching power supplies is very important, and sometimes critical for proper function. Poor layout design can result in poor line or load regulation and stability issues. Please follow these guidelines and take Figure 3 as reference:

1) The high current paths (GND, VIN and SW) should be placed very close to the device with short, direct and wide traces.

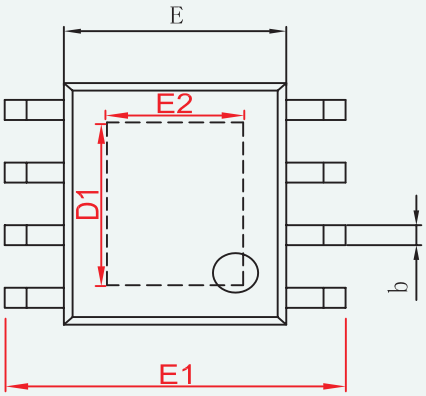
2) The input capacitor needs to be as close as possible to the VIN and GND pins.

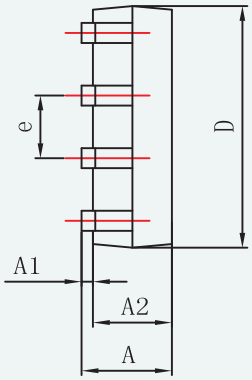
3) The external feedback resistors should be placed next to the FB pin.

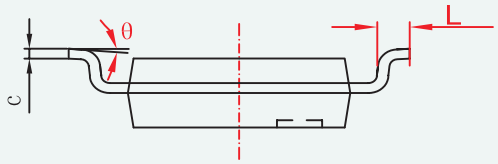
4) Keep the switching node SW short and away from the feedback network.

Package Information

CS5525E ESOP8L







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Notes:

(1) All dimensions are in millmeters

(2) Comples with standard JEDEC MO-187