集成Charge pump,3VRMS音频线性驱动器
3VRMS Audio Line Driver with Integrated Charge Pump

概要

IU632C是一款3VRMS无杂音立体声线性驱动器,此驱动器设计用于去除输出隔直流电容器，以减少组件数目及成本。对于那些将尺寸和成本作为关键设计参数的单电源电子产品，该器件是理想的选择,IU632C能够在3.3V/5.0V电源电压供电时驱动2VRMS/3VRMS进入一个10kΩ 负载。此器件具有差分输入，并采用外部增益设置电阻以支持±1V至±10V的增益范围，而且可为每个通道单独配置增益。线路输出只需要使用一个简单的电阻器-电容器ESD 保护电路即可。IU632C 具有针对无杂音音频打开/关闭控制的内置有源静音控制功能.IU632C具有一个外部欠压检测器，该欠压检测器在电源被移除时将输出静音，从而确保了无杂音的关断操作。与产生2VRMS/3VRMS 输出的传统方法相比,在音频产品中使用IU632C能够大幅度地减少组件数量.IU632C 既不需要采用一个高于3.3V /5V的电源来产生其5.6Vpp/8.5Vpp 输出，也不需要一个分离轨电源.IU632C 内部集成了电荷泵以产生一个负电源轨，此负电源轨可提供一个良好的无杂音接地偏置2VRMS 输出。IU632C采用14引脚TSSOP14L 封装。

封装

- TSSOP14

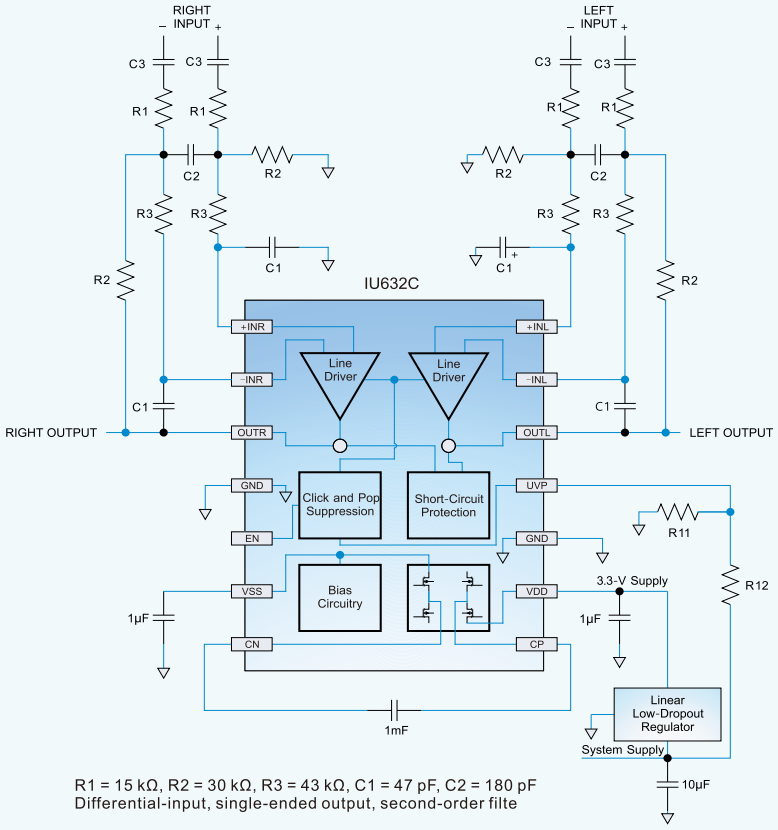
描述

- 在由3.3V电源供电时,2Vrms 进入2.5KΩ 负载
- 在由5V电源供电时,3Vrms 进入2.5KΩ 负载
- 2Vrms 进入2.5kΩ 负载时,(THD)+N < 0.01%
- 高信噪比(SNR)> 90dB
- 可支持600Ω 输出负载
- 差分输出和单端输出
- 由外部增益设定电阻器实现的可调增益
- 低直流偏移：< 1mV
- 接地基准输出免除了对隔直电容的需要
  --省元件，降低了成本
  --改善了THD+N性能
  --提升了输出的低频响应性能
- 短路保护功能,外部欠压静音
- 瞬时杂音(喀哒声和噼啪声)抑制电路
- 用于实现无杂音音频打开/关闭控制的有源静音控制

应用

- 网络机顶盒,电视机,DVD 播放器
- 麦克风
- 微型组合音响系统
- 声卡
- 笔记本电脑

典型应用图



R1 = 15 kΩ, R2 = 30 kΩ, R3 = 43 kΩ, C1 = 47 pF, C2 = 180 pF
Differential-input, single-ended output, second-order filte

3VRMS Audio Line Driver with Integrated Charge Pump

General Description

The IU632C is a 3VRMS pop-free stereo line driver designed to allow the removal of the output dcblocking capacitors for reduced component count and cost. The device is ideal for single-supply electronics where size and cost are critical design parameters.The IU632C is capable of driving 3VRMS into a 2.5kΩ load with 5V supply voltage. The device has differential inputs and uses external gain setting resistors to support a gain range of ±1V/V to ±10V/V, and gain can be configured individually for each channel. Line outputs requiring just a simple resistor-capacitor ESD protection circuit. The IU632C has built-in active-mute control for pop-free audio on/off control. The IU632C has an external undervoltage detector that mutes the output when the power supply is removed, ensuring a pop-free shutdown.Using the IU632C in audio products can reduce component count considerably compared to traditional methods of generating a 3VRMS output. The IU632C does not require a power supply greater than 3.3 V to generate its 5.6-Vpp output and 5 V to generate its 8.5-Vpp output, nor does it require a split-rail power supply. The IU632C integrates its own charge pump to generate a negative supply rail that provides a clean, pop-free ground-biased 3VRMS output.

Package

- TSSOP14

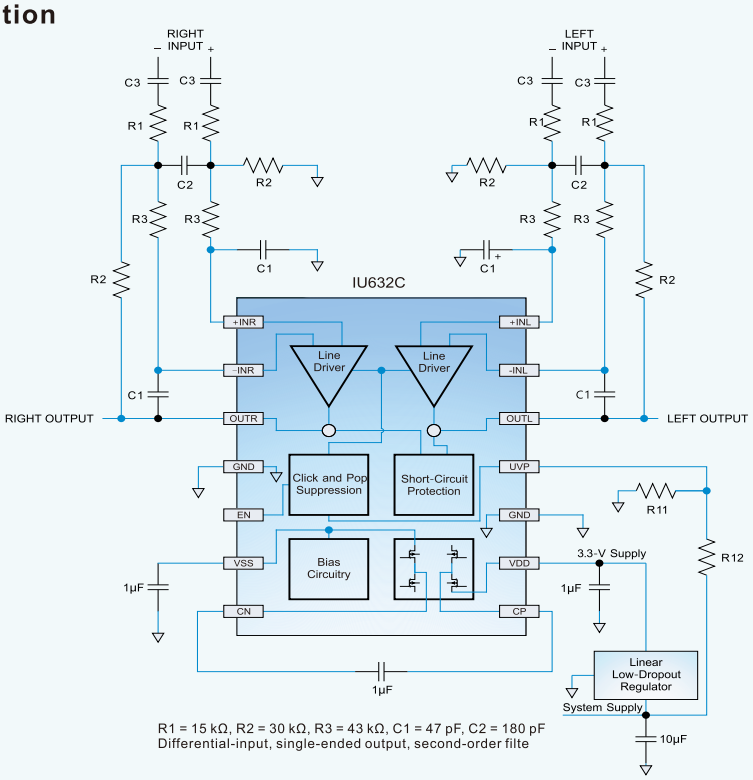
Features

- 2Vrms Into 2.5 kΩ With 3.3V Supply
- 3Vrms Into 2.5 kΩ With 5V Supply
- Low THD+N < 0.01% at 2Vrms Into 2.5 kΩ
- High SNR, >90 dB
- 600Ω Output Load Compliant
- Differential Input and Single-Ended Output
- Adjustable Gain by External Gain-Setting Resistors
- Low DC Offset, <1 mV
- Ground-Referenced Outputs Eliminate DCBlocking Capacitors
  - Reduce Board Area,Reduce Component Cost
  - Improve THD+N Performance
  - No Degradation of Low-Frequency Response Due to Output Capacitors
- Short-Circuit Protection
- Click- and Pop-Reduction Circuitry
- External Undervoltage Mute
- Active Mute Control for Pop-Free Audio On/Off Control

Applications

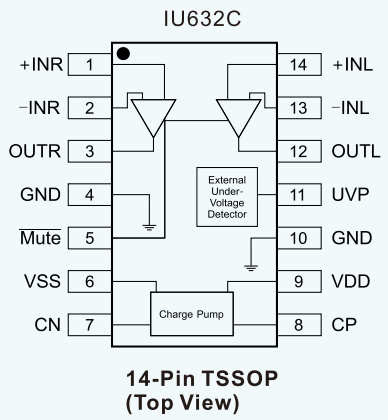
- Notebooks
- Sound Cards
- Set-Top Boxes.LCD TV
- Mini/Micro Combo Systems
- Laptops
- Microphone

Typical Application



R1 = 15 kΩ, R2 = 30 kΩ, R3 = 43 kΩ, C1 = 47 pF, C2 = 180 pF
Differential-input, single-ended output, second-order filte

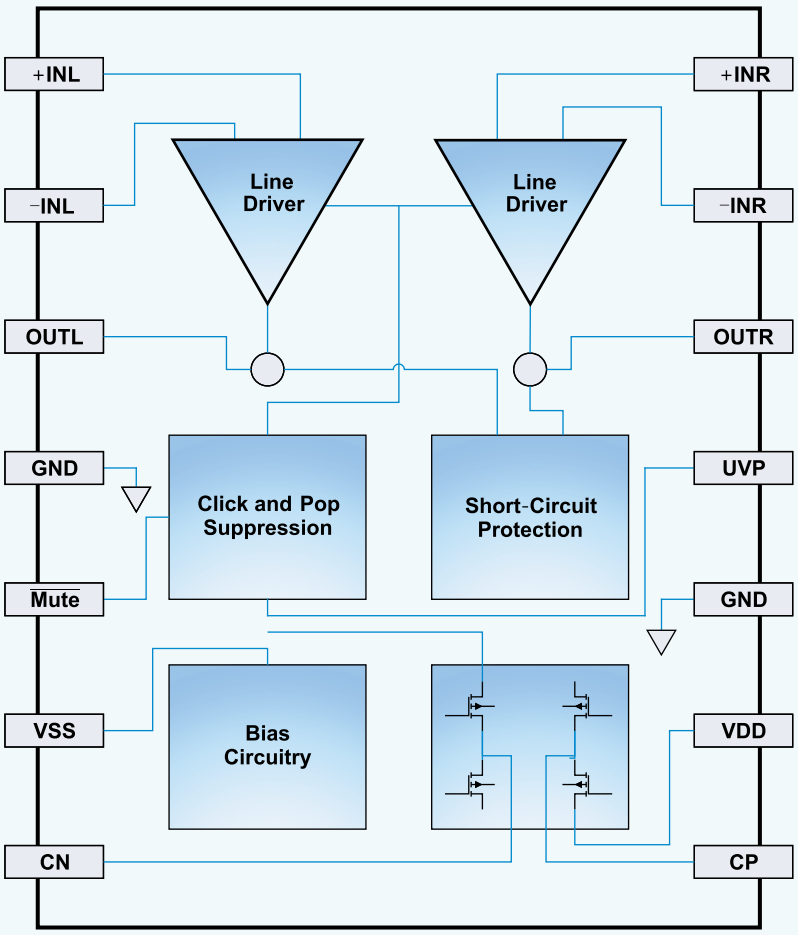
Pin Configuration and Functions



14-Pin TSSOP
(Top View)

PIN		TYPE	DESCRIPTION
NAME	NO.		
CN	7	I/O	Charge-pump flying capacitor negative connection
CP	8	I/O	Charge-pump flying capacitor positive connection
GND	4,10	P	Ground
−INL	13	I	Left-channel OPAMP negative input
+INL	14	I	Left-channel OPAMP positive input
−INR	2	I	Right-channel OPAM Pnegative input
+INR	1	I	Right-channel OPAMP positive input
$\overline{\text{Mute}}$	5	I	Mute,active-low
OUTL	12	O	Left-channel OPAMP output
OUTR	3	O	Right-channel OPAMP output
UVP	11	I	Under voltage protection,internal pullup Unconnected if UVP function is unused.
VDD	9	P	Positive supply
VSS	6	P	Negative voltage generated by charge pump

Functional Block Diagram



Absolute Maximum Ratings

		MIN	MAX	UNIT
	Supply voltage,VDD to GND	−0.3	6	V
V_I	Input voltage	V_{SS} −0.3	VDD+0.3	V
R_L	Minimum load impedance – line outputs – OUTL, OUTR	600		Ω
	$\overline{\text{Mute}}$ to GND,UVP to GND	−0.3	VDD+0.3	V
T_J	Maximum operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−40	150	°C

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	DC supply voltage	2.5		5.5	V
R_L	Load impedance		0.6	10		kΩ
V_{IL}	Low-level input voltage	$\overline{\text{Mute}}$		40		% of VDD
V_{IH}	High-level input voltage	$\overline{\text{Mute}}$		60		% of VDD
T_A	Operating free-air temperature		−40	25	85	°C

Thermal Information

THERMALMETRIC		TSSOP14	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	49	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62	°C/W

Ordering and Marking Information

Device	Package Type	Device Marking	Reel Size	Tape Width	Quantity
IU632C	TSSOP14		13''	12mm	4000 units

ESD Susceptibility

ESD Susceptibility-HBM ---------- ±8kV

ESD Susceptibility-MM ---------- ±2000V

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device.Functional operation at conditions other than the operating conditions specified is not implied.Only one Absolute Maximum Rating should be applied at one time.

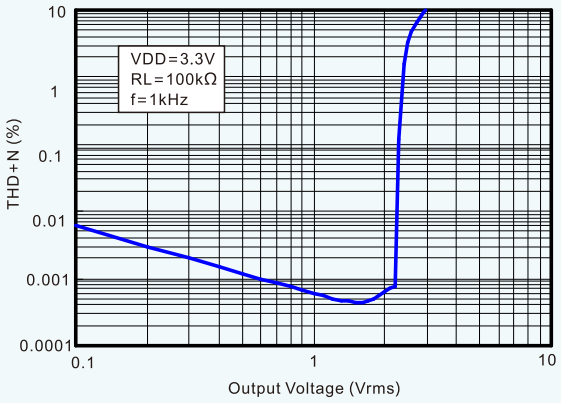
Electrical Characteristics

PVDD=3.3V, T_A=25℃J, R_L=2.5kΩ, C_{FLY}=C_{PVSS}=1μF, C_{IN}=1μF, R_I=10kΩ, R_F=20kΩ (unless otherwise noted)

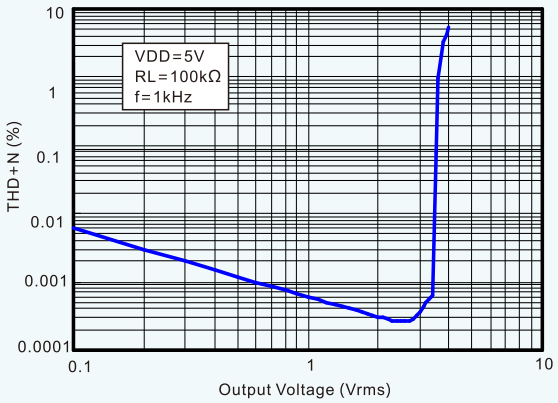
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage Range		2.5		5.5	V
V_{OS}	Output Offset Voltage	Input grounded, unity gain.	-4		4	mV
I_Q	Quiescent Current	No load		4.6		mA
$I_{Q(off)}$	Supply Current in Shutdown				0.33	mA
V_O	Output Voltage	V_{DD}=3.3V, f=1kHz, THD=1%	2.05			V_{RMS}
		V_{DD}=5V, f=1kHz, THD=1%	3.05			V_{RMS}
THD+N	Total Harmonic Distortion Plus Noise	V_O=3V_{RMS}, f=1kHz		0.001		%
V_{ENH}	High-level Threshold Voltage(EN)	V_{DD}=3.3V, EN Low to High Transition	1			V
		V_{DD}=5V, EN Low to High Transition	1			V
V_{ENL}	Low-level Threshold voltage(EN)	V_{DD}=3.3V, EN High to Low Transition			0.5	V
		V_{DD}=5V, EN High to Low Transition			0.6	V
$\|I_{ENH}\|$	High-level input current(EN)	V_{DD} = 5 V, V_I = V_{DD}			0.1	μA
$\|I_{ENL}\|$	Low-level input current(EN)	V_{DD} = 5 V, V_I = 0 V			1	μA
X_{TALK}	Crosstalk	V_O=3V_{RMS}, f=1kHz		-96		dB
I_{SC}	Short Circuit Current	V_{DD}=5V		90		mA
R_{IN}	Input Resistor Range		1	10	47	kΩ
SR	Slew Rate			5		V/μs
C_L	Maximum Capacitive Load				470	pF
CF	Flying Capacitor		0.1	0.33	2.2	μF
V_N	Noise Output Voltage	BW=20Hz to 20kHz		4.3		μV_{RMS}
SNR	Signal to Noise Ratio	V_O=3V_{RMS}, f=1kHz, BW=20kHz		117		dB
GBW	Unity Gain Bandwidth	No load		10		MHz
A_{VOL}	Open-Loop Voltage Gain	No load		130		dB
V_{UVP}	External Under-voltage Detection	V_{DD}=3.3V	1.15	1.20	1.25	V
		V_{DD}=5V	1.16	1.21	1.28	V
I_{HYS}	External Under-voltage Detection Hysteresis Current			4.5		μA
f_{CP}	Charge Pump Frequency			300		kHz

Typical Performance Characteristics

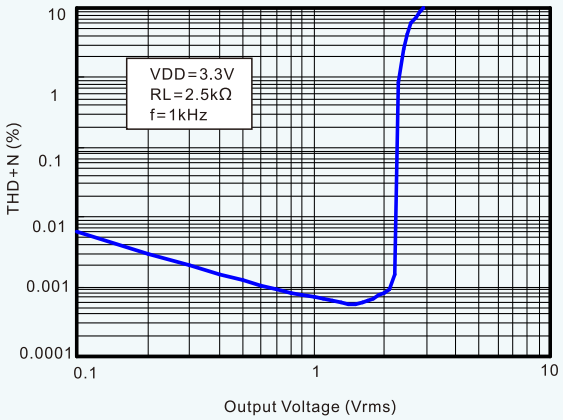
Total Harmonic Distortion + Noise vs. Output Voltage



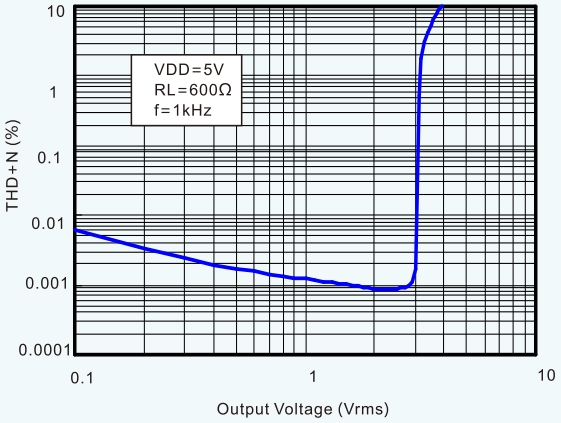
Total Harmonic Distortion + Noise vs. Output Voltage



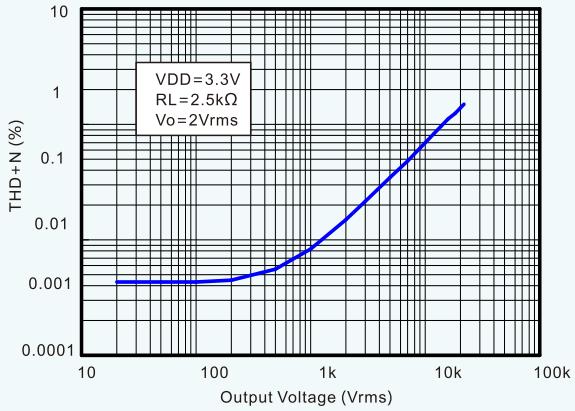
Total Harmonic Distortion + Noise vs. Output Voltage



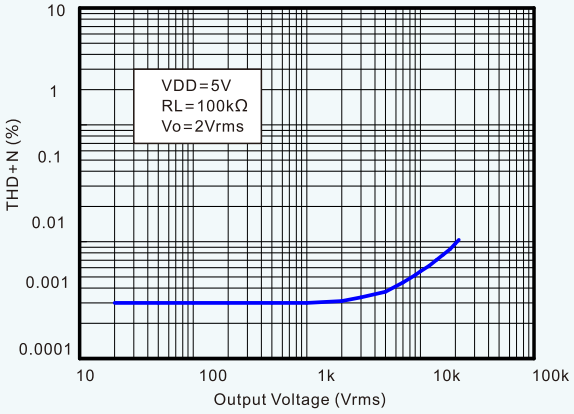
Total Harmonic Distortion + Noise vs. Output Voltage



Total Harmonic Distortion + Noise vs. Frequency



Total Harmonic Distortion + Noise vs. Frequency



Application Information

IU632C operates from a single supply voltage PVDD.

It integrated charge pump generates a negative supply −PVDD at the VSS pin. The Line driving amplifiers work with dual supplies: PVDD and −PVDD. Therefore, the DC level of the audio output can be designed to be 0V. A DC-blocking capacitor typically seen in a single-supplied driver is not necessary.The supply range of the IU632C is 2.5V to 5.5V. For a 3VRMS output, the recommended supply voltage is 5V. For a 2VRMS output, the recommended supply voltage is 3.3V.RIN of 2.5k and RFB of 5k set the inverting gain of 2. Because of the exceptional noise performance of IU632C, the dominant noise source is actually from RIN. To get better noise performance, lower inputresistance and feedback resistance may be used.

Integrated Charge Pump

The integrated charge pump in IU632C generates negative power supply from a single supply PVDD. Aflying capacitor for the charge pump shall be applied between CP and CN. At the same time a decoupling capacitorshall be applied between PVSS and ground. Typical value for the flying capacitor is 0.33uF.Typical value of thedecoupling capacitor shall be same as or larger than that of the flying capacitor. Low-ESR capacitors arerecommended for the flying capacitor and the decoupling capacitor.

Audio Signal Amplification Gain Setting

The main application of the IU632C is to amplify/buffer audio signals and drive audio lines with very lowdistortion. Typical application circuits with inverting gain are shown in Figure a.Non-inverting amplification of audio signals is also possible with same low distortion.

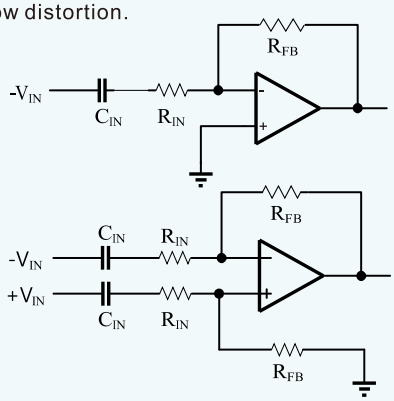


Figure a Typical Application Circuit of IU632C

AC-Coupling Input Capacitors

Because of the integrated charge pump that generates negative rail, IU632C may be used to amplify audio signal so the output DC voltage is 0V. This usually requires the DC voltage of the input signal to be 0V. If the input signal has a DC level other than 0V, an AC-coupling capacitor is necessary to block the DC voltage.The AC-coupling capacitor essentially forms a high-pass filter at the input. The cut-off frequency of the filter has to below enough not to distort the input audio signal. For an inverting amplifier shown in Figure a the cut-off frequency may be calculated as following:

$$f_c = \frac{1}{2\pi R_{in} C_{in}}$$

Adding Low-Pass Filtering to the Gain

If low-pass filtering is necessary in addition to the audio signal amplification, a second-order filter can be implementedas shown in Figure b. Choice of C3, R1, R2, and R3 is based on the gain setting requirement and AC-coupling cut-off frequency as discussed above. C1, C2 and C4 may be calculated depending on the bandwidth. Example choices of R and C are listed in Table 1. If first-order filtering satisfies performance requirements, simply remove the C2 and C4 to lower the component counts.

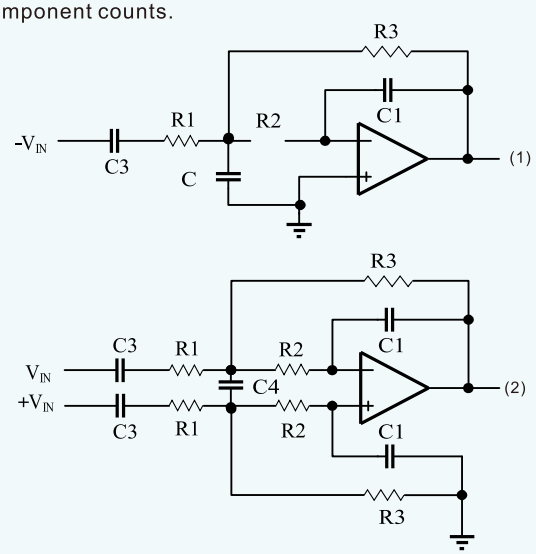


Figure b Second-order filter with gain: (1) Single-ended input; (2) Differential input

Table 1 Example RC setting at different gains

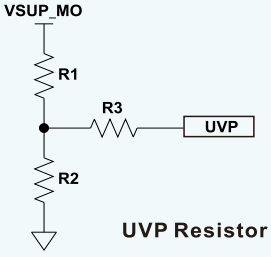
Gain	R1	R2	R3	C1	C2	C3	C4
G=2	2.5k	2.5k	10k	120pF	1nF	2.2uF	360pF
G=2.5	2.4k	2.4k	12k	91pF	750pF	2.2uF	390pF
G=3.75	2k	2k	15k	75pF	750pF	4.7uF	390pF

External Undervoltage Detection

External undervoltage detection can be used to mute/shut down the IU632C before an input device can generate a pop.The shutdown threshold at the UVP pin is 1.2V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application. The thresholds can be determined as follows:

$V_{UVP} = 1.2 \times (R1+R2)/R2$

Hysteresis = $4.5\mu A \times R3 \times (R1+R2)/R2$



UVP Resistor Divider

Driving Large Capacitive Load

IU632C is designed to drive large capacitive loads up to 220pF directly. When driving larger capacitive loads with the IU632C, a small series resistor at the output (RISO in Figure c) improves the feedback loop' s phase margin and stability by making the output load resistive at higher frequencies. Usually RISO of 50Ω is sufficient.

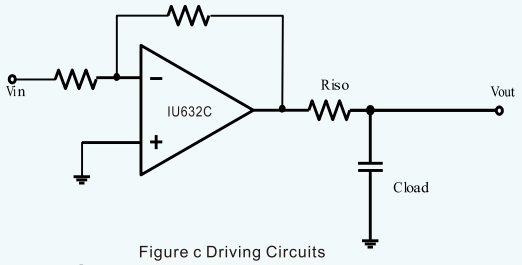


Figure c Driving Circuits

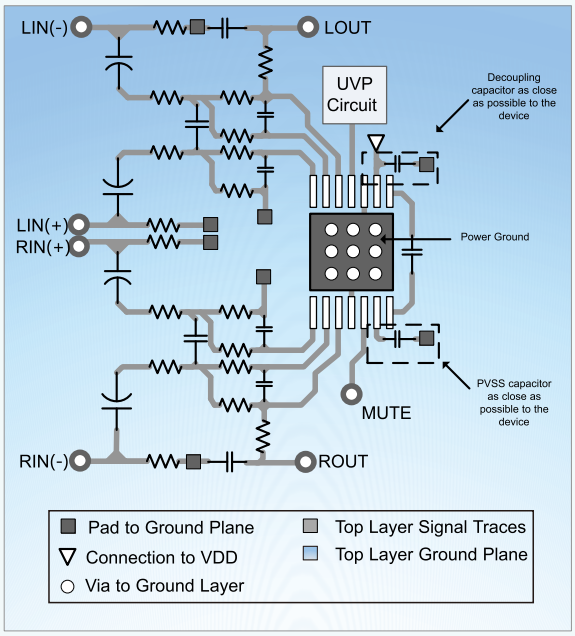
Power Supply Layout and Bypass

The power supply pin of IU632C should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts. Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place externalcomponents as close to the op amps' pins as possible.

Proper Board Layout

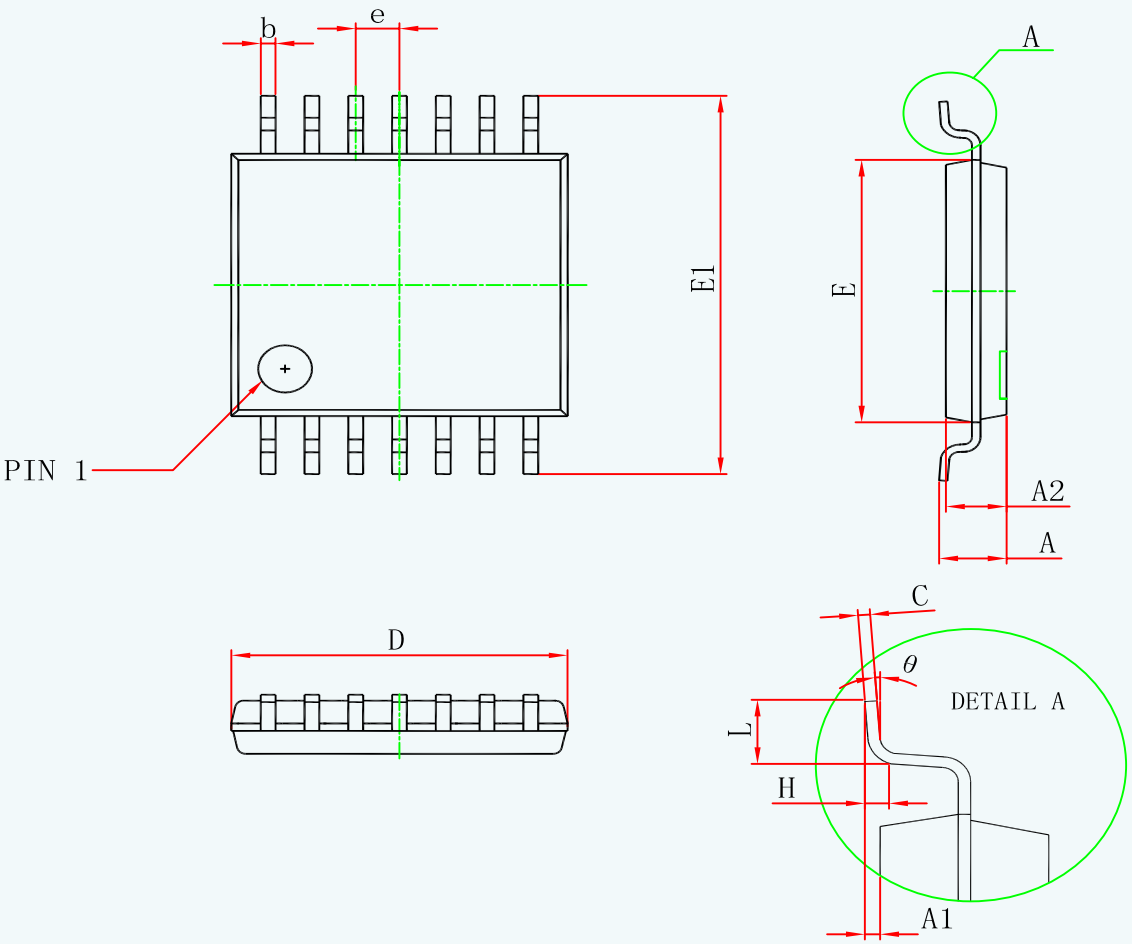
To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board. Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling. A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Layout Example



Package Information

IU632C TSSOP14 PACKAGE OUTLINE DIMENSIONS UNITS:mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

MOS电路操作注意事项：

静电在很多地方都会产生，采取下面的预防措施，可以有效防止MOS 电路由于受静电放电影响而引起的损坏：

- 操作人员要通过防静电腕带接地。
- 设备外壳必须接地。
- 装配过程中使用的工具必须接地。
- 必须采用导体包装或抗静电材料包装或运输。

声明:

- 上海埃诚攸微电子有限公司保留说明书的更改权，恕不另行通知！客户在使用前应获取最新版本资料，并验证相关信息是否完整和最新。
- 任何半导体产品在特定条件下都有一定的失效或发生故障的可能，买方有责任在使用上海埃诚攸微电子有限公司产品进行系统设计和整机制造时遵守安全标准并采取安全措施，以避免潜在失败风险可能造成人身伤害或财产损失情况的发生！
- 产品品质的提升永无止境，上海埃诚攸微电子有限公司将竭诚为客户提供更优秀的产品！