ACM3220 36mW Stereo Headphone Amplifier With Low Power Dissipation

1. Features

- Wide Power Supply Range: 2.5V to 5.5V
- Gain Settings: -6dB, 0dB, 3dB, and 6dB
- High Power Supply Noise Rejection
  - 100 dB PSRR at 217 Hz
  - 90 dB PSRR at 10kHz
- Eliminates Need for DC-Blocking Capacitors
  - Outputs Biased at 0V
  - Improves System Noise Performance
- Fully Differential or Single-Ended Inputs
  - Built-In Resistors Reduces Component Count
  - Improves System Noise Performance
- Short-Circuit and Thermal-Overload Protection
- 2.3 mA Typical Supply Current
- Constant Maximum Output Power from 2.5V to 5.5V
- Active Click and Pop Suppression
- ±8 kV HBM ESD Protected Outputs
- Small Package Available
  - 16-Pin, 3 mm × 3mm Thin QFN

2. Applications

- Notebook PCs
- Cellular Phones
- PDAs
- Smart Phones
- Portable Audio Equipment
- MP3 Players

3. General Description

The ACM3220 is a stereo headphone amplifier that eliminates the need for external dc-blocking output capacitors. Differential stereo inputs and built-in resistors. Differential stereo inputs and built-in resistors set the device gain, further reducing external component count. Gain is selectable at -6dB, 0dB, 3dB or 6dB. The amplifier drives 36mW into 32Ω speakers from a single 3.6V supply. The ACM3220 provides a constant maximum output power independent of the supply voltage, thus facilitating the design for prevention of acoustic shock.

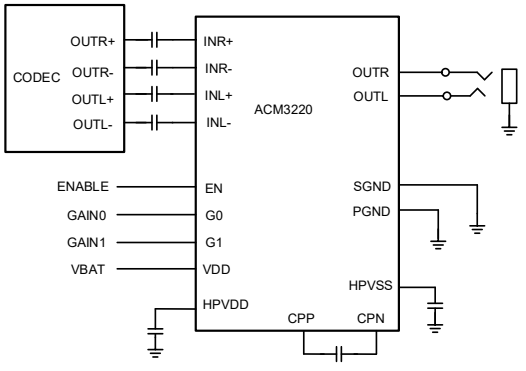
The ACM3220 features fully differential inputs to reduce system noise pickup between the audio source and the headphone amplifier. The high power supply noise rejection performance and differential architecture provides increased RF noise immunity. For single-ended input signals, connect INL+ and INR+ to ground.

The device has built-in pop suppression circuitry to completely eliminate disturbing pop noise during turn-on and turn-off. The amplifier outputs have short-circuit and thermal-overload protection along with ±8 kV HBM ESD protection, simplifying end equipment compliance to the IEC 61000-4-2 ESD standard.

The ACM3220 operates from a single 2.5V to 5.5V supply with 2.3mA of typical supply current. Shutdown mode reduces supply current to less than 1μA.

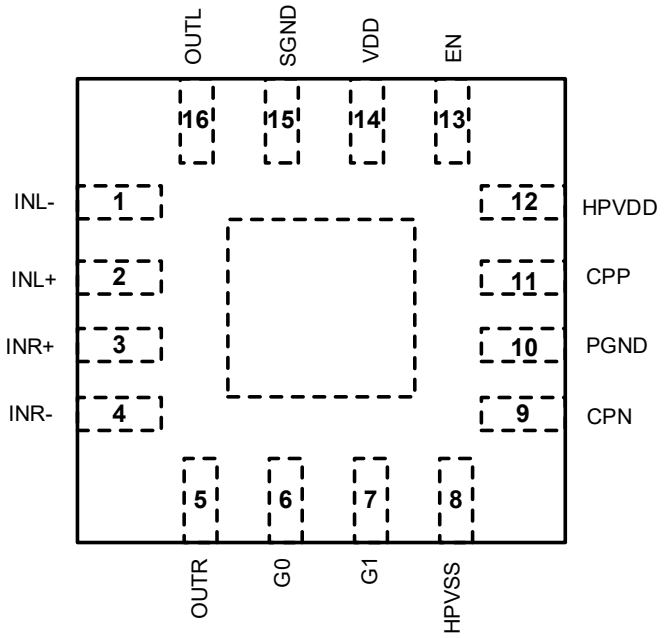
4. Device Information

Part number	Package	Body size
ACM3220	QFN (16)	3 mm × 3 mm



5. Pin Configuration and Function Descriptions

QFN Package
(Top View)



Pin No.	Name	Type	Description
1	INL-	I	Inverting left input for differential signals; left input for single-ended signals
2	INL+	I	Non-inverting left input for differential signals. Connect to ground for single-ended input applications
3	INR+	I	Non-inverting right input for differential signals. Connect to ground for single-ended input applications.
4	INR-	I	Inverting right input for differential signals; left input for single-ended signals
5	OUTR	O	Right headphone amplifier output. Connect to right terminal of headphone jack
6	G0	I	Gain select
7	G1	I	Gain select
8	HPVSS	P	Charge pump output and negative power supply for output amplifiers; Connect 1μF capacitor to GND
9	CPN	P	Charge pump negative flying cap. Connect to negative side of 1μF capacitor between CPP and CPN
10	PGND	P	Ground
11	CPP	P	Charge pump positive flying cap. Connect to negative side of 1μF capacitor between CPP and CPN
12	HPVDD	P	Positive power supply for headphone amplifiers. Connect to a 2.2uF capacitor. Do not connect to VDD
13	EN	I	Amplifier Enable. Connect to Logic low to shutdown; Connect to logic high to acitvate
14	VDD	P	Positive power supply for ACM3220
15	SGND	P	Amplifier reference voltage. Connect to ground terminal of headphone jack
16	OUTL	O	Left headphone amplifier output. Connect to left terminal of headphone jack

Thermal Pad	-		Solder the exposed metal pad on the ACM3220 QFN package to the landing pad on the PCB. Connect the landing pad to ground or leave it electrically unconnected (floating)

6. Device Family Comparison

Device Name	VDD	Output Power
ACM3220	2.5V ~ 5.5V	36mW into 32Ω

7. Specifications

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Supply Voltage	VDD	-0.3	6	V
Headphone amplifier Supply Voltage	HPVDD (do not connect to external supply)	-0.3	2	V
Input voltage, V_I	INR+, INR-, INL+, INL-	HPVSS-0.3	HPVDD+0.3	V
	EN, G0, G1	-0.3	VDD+0.3	V
Operating free-air temperature range, T_A		-40	85	℃
Operating junction temperature range, T_J		-40	150	℃
T_{stg}	Storage temperature	-60	85	℃

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	OUTL, OUTR	+/- 8000	V
			All Other Pins	+/- 2000	
		Charged-device model (CDM),per JEDEC specification JESD22-C101, all pins(2)		+/- 1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply Voltage, VDD		2.5		5.5	V
V_{IH}	High-level input voltage; EN, G0, G1	1.3			
V_{IL}	Low-level input voltage; EN, G0, G1			0.6	V
V_I	Input voltage; INR+, INR-, INL+, INL-	0		HPVDD+0.3	V
	Voltage applied to Output; OUTR, OUTL (when EN = 0V)	-0.3		3.6	V
T_A	Ambient Operating Temperature	-40		85	℃

7.4 Thermal Information

THERMAL METRIC		QFN 16 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	51.1	℃/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	53.9	
$R_{\Theta JB}$	Junction-to-board thermal resistance	24.3	
Ψ_{JT}	Junction-to-top characterization parameter	0.9	
Ψ_{JB}	Junction-to-board characterization parameter	24.3	
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.0	

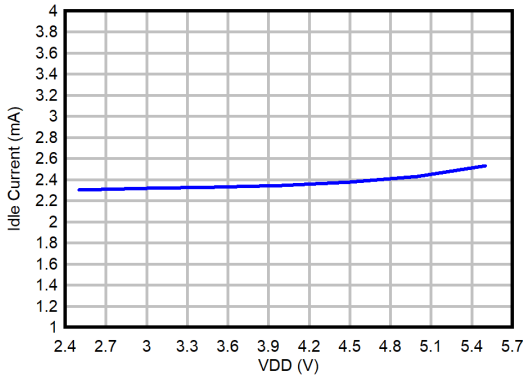
7.5 Electrical Characteristics

Free-are room temperature 25° C , V_{DD} = 3.6 V, T_A = 25 °C, R_L = 16 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output offset voltage			-2		2	mV
Power supply rejection ratio		V_{DD}=2.5 V to 5.5 V		100		dB
High-level output current (EN, G0, G1)					1	μA
Low-level output current (EN, G0,G1)					1	
Supply Current		V_{DD}=2.5 V, No load, EN = V_{DD}		2.3		mA
		V_{DD}=3.6 V, No load, EN = V_{DD}		2.32		
		V_{DD}=5.5 V, No load, EN = V_{DD}		2.43		
		EN = 0 V, V_{DD} = 2.5V to 5.5V		0.55	1.35	μA
AMPLIFIER OPERATING MODE AND DC PARAMETERS						
P_O	Output power (1) (Outputs in phase)	THD = 1%, f = 1 kHz, R_L = 32Ω		36		mW
		THD = 1%, f = 1kHz, R_L = 16Ω		27		
V_O	Output voltage (1) (Outputs in phase)	THD = 1%, V_{DD} = 3.6 V, f = 1 kHz, R_L = 100Ω		1		V_{RMS}
A_V	Closed-loop voltage gain (OUT / IN-)	G0 = 0 V, G1 = 0 V, (-6dB)		-0.5		V/V
		G0 ≥ 1.3 V, G1 = 0 V, (0dB)		-1.0		
		G0 ≥ 0 V, G1 ≥ 1.3 V, (3dB)		-1.41		
		G0 ≥ 1.3 V, G1 ≥ 1.3 V, (6dB)		-2.0		
ΔA_V	Gain matching	Between Left and Right channels		1%		
R_{IN}	Input impedance (per input pin)	G0 = 0 V, G1 = 0 V, (-6dB)		26.4		kΩ
		G0 ≥ 1.3 V, G1 = 0 V, (0dB)		19.8		
		G0 ≥ 0 V, G1 ≥ 1.3 V, (3dB)		16.5		
		G0 ≥ 1.3 V, G1 ≥ 1.3 V, (6dB)		13.2		
	Input Impedance in shutdown (per input pin)	EN = 0 V		0.3		
V_{CM}	Input common-mode voltage range		-0.5		1.5	V
	Output impedance in shutdown			0.25		kΩ
	Input-to-output attenuation in shutdown	EN = 0 V		80		dB
PSRR	AC-power supply rejection ratio	200 mV_{pp} ripple, f = 217 Hz		-100		dB
		200 mV_{pp} ripple, f= 10 kHz		-90		
THD+N	Total Harmonic distortion plus noise	P_O = 20 mW into 16Ω, f = 1 kHz, V_{DD}=3.6V		0.011		%
		P_O = 25 mW into 32Ω, f = 1 kHz, V_{DD}=3.6V		0.007		%
SNR	Signal-to-noise ratio	P_O = 20mW; G0 ≥ 1.3V, G1 = 0 V, (A_V = 0 dB)		100		dB
E_n	Noise output voltage	A-weighted, (A_V = -6 dB)		4.5		μV_{RMS}
		A-weighted, (A_V = 0 dB)		6		μV_{RMS}
f_{OSC}	Charge pump switching frequency		470	500	510	kHz
t_{ON}	Start-up time from shutdown			5		ms
	Crosstalk	P_O = 20 mW, f = 1 kHz		-80		dB
	Thermal shutdown	Threshold		150		°C
		Hysteresis		29		°C

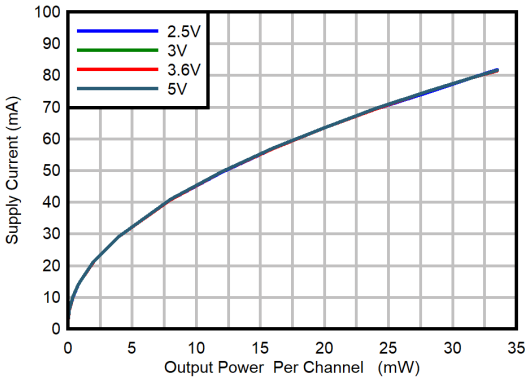
8. Typical Characteristics

TA = 25 °C, V_{DD} = 3.6V, Gain = 0 dB, EN = 3.6 V, C_{HPVDD} = C_{HPVSS} = 2.2 μF, C_{INPUT} = C_{FLYING} = 1μf, Outputs in Phase.



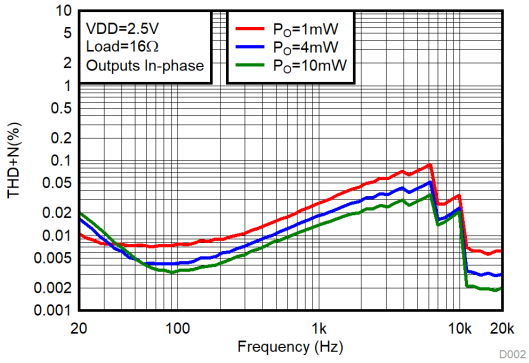
(No Load, No Audio Playing)

Figure 1 Idle Current vs VDD



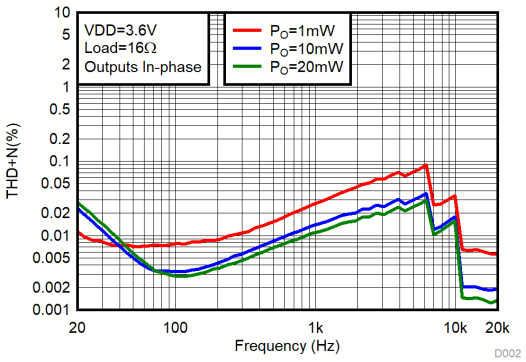
(Load=16Ω, Outputs In-phase)

Figure 2 Supply Current vs Output Power



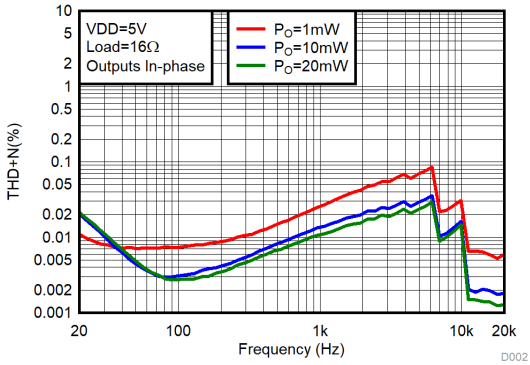
(Load=16Ω, VDD=2.5V)

Figure 3 THD+N vs Frequency



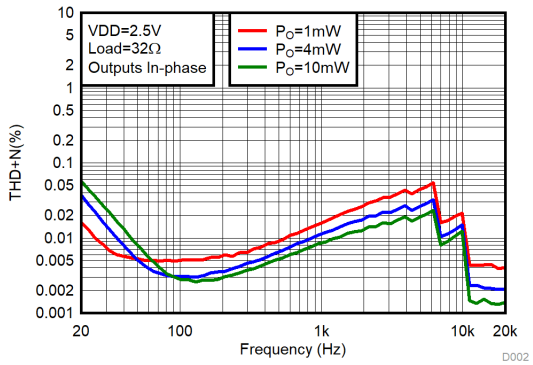
(Load=16Ω, VDD=3.6V)

Figure 4 THD+N vs Frequency



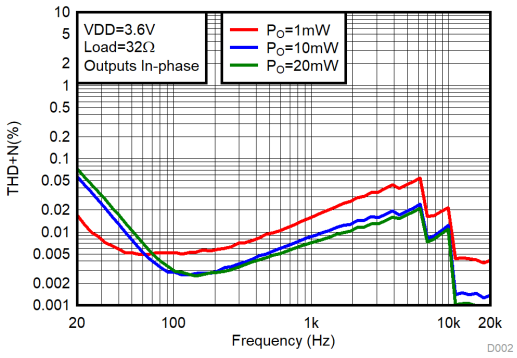
(Load=16Ω, VDD=5V)

Figure 5 THD+N vs Frequency



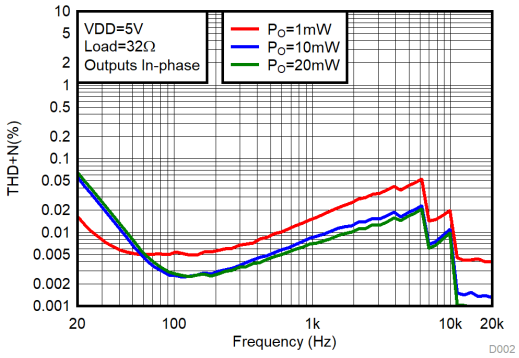
(Load=32Ω, VDD=2.5V)

Figure 6 THD+N vs Frequency



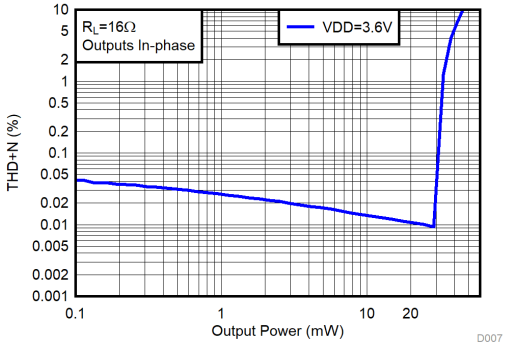
(Load=32Ω, VDD=3.6V)

Figure 7 THD+N vs Frequency



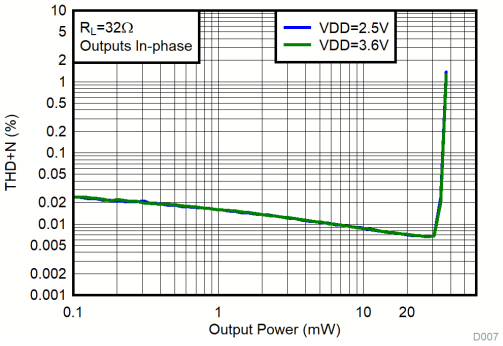
(Load=32Ω, VDD=5V)

Figure 8 THD+N vs Frequency



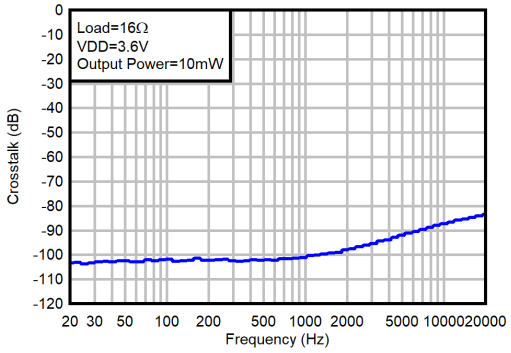
(Load=16Ω, Outputs In-phase)

Figure 9 THD+N vs Output Power



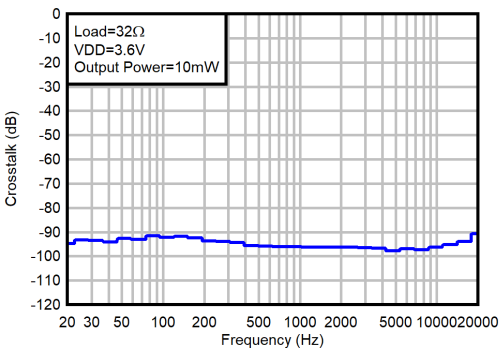
(Load=32Ω, Outputs In-phase)

Figure 10 THD+N vs Output Power



(Load=16Ω, Outputs In-phase)

Figure 11 Crosstalk



(Load=32Ω, Outputs In-phase)

Figure 12 Crosstalk

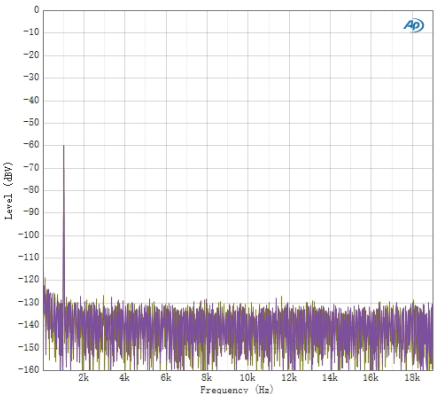


Figure 13 Output Spectrum vs Frequency

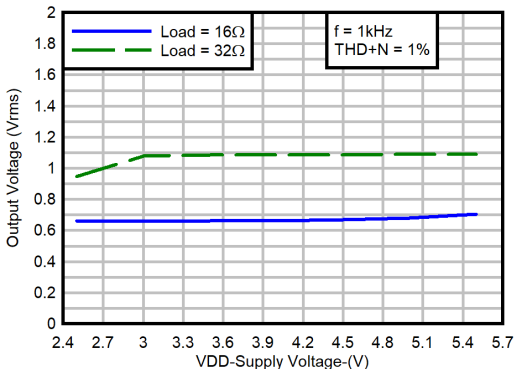


Figure 14 Output Voltage vs Supply Voltage

9. Detailed Description

9.1 Overview

The ACM3220 is a stereo headphone amplifier that requires no output DC blocking capacitors and is capable of delivering 27mW/Ch into 16-Ω speakers. The device has built-in pop suppression circuitry to completely eliminate pop noise during turn-on and turn-off. The amplifier outputs have short-circuit and thermal-overload protection.

The ACM3220 features fully differential inputs to reduce system noise pickup between the audio source and the headphone amplifier. The high power supply noise rejection performance and differential architecture provides increased RF noise immunity.

Differential stereo inputs and built-in resistors set the device gain, reducing external component count. The ACM3220 has four gain settings which are controlled with pin G0 and G1. The combination of these pins set the device to -6dB, 0dB, 3dB or 6dB gain.

The ACM3220 operates from a single 2.5V to 5.5V supply with 2.3mA of typical supply current, as it uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers. Shutdown mode reduces supply current to less than 1.35uA.

9.2 Functional Block Diagram

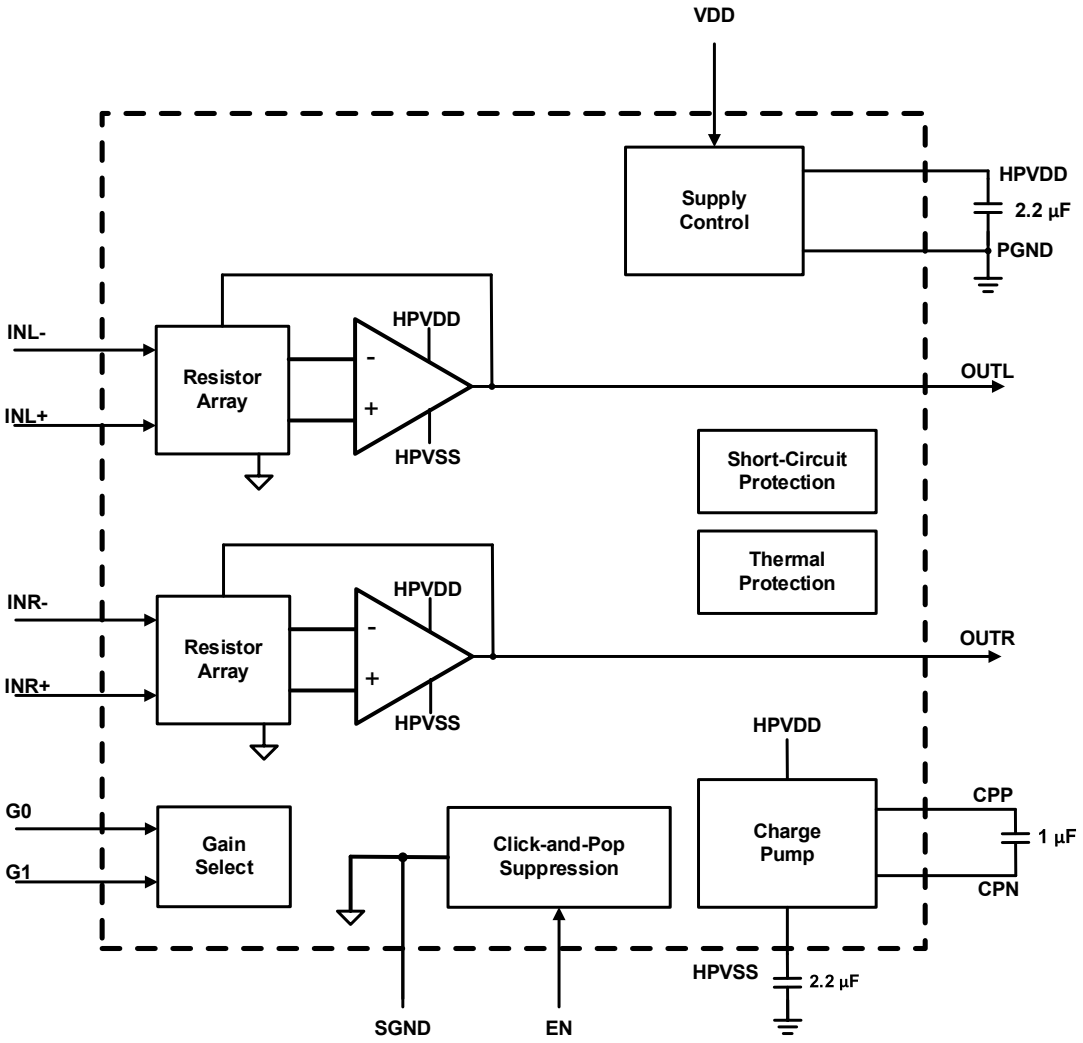


Figure 15 Function Block Diagram

9.3 Feature Description

9.3.1 Headphone Amplifiers

Single-supply headphone amplifiers typically require dc-blocking capacitors to remove dc bias from their output voltage. If DC bias is not removed, large DC current will flow through the headphones which wastes power, clip the output signal, and potentially damage the headphones.

These DC-blocking capacitors are often large in value and size. Headphone speakers have a typical resistance between 16Ω and 32Ω. This combination creates a high-pass filter with a cutoff frequency as shown in Equaltion 1, where R_L is the load impedance, C_O is the DC block capacitor, and f_C is the cutoff frequency.

$$f_C = \frac{1}{2\pi R_L C_O} \quad (1)$$

For a given high-pass cutoff frequency and load impedance, the required dc-blocking capacitor is found as:

$$C_O = \frac{1}{2\pi R_L f_C} \quad (2)$$

Reducing f_C improves low frequency fidelity and requires a larger dc-blocking capacitor. To achieve a 20Hz cutoff with 16Ω headphones, C_O must be at least 500μF. Large capacitor values require large packages, consuming PCB area, increase height, and increasing cost of assembly. During start-up or shutdown the dc-blocking capacitor has to be charged or discharged. This causes an audible pop on start-up and power-down Large dc-blocking capacitors also reduce audio output signal fidelity.

Two different headphone amplifier architectures are available to eliminate the need for dc-blocking capacitors. The capless amplifier architecture is similar provides a reference voltage to the headphone connector shield pin as shown in Figure 16. The audio output signal are centered around this reference voltage, which is typically half of the supply voltage to allow symmetrical output voltage swing.

When using a capless amplifier do not connect the headphone jack shield to any ground reference or larger currents will result. This makes capless amplifiers ineffective for plugging non-headphone accessories into the headphone connector. Capless amplifier are useful only with floating GND headphones.

ACM3220 operates from a single supply voltage and uses an internal charge pump to generate a negative supply rail for the headphone amplifier. The output voltages are centered around 0V and are capable of positive and negative voltage swings as shown in Figure 16. ACM3220 requires no output dc-blocking capacitors. The headphone connector shield pin connects to ground and will interface will headphones and non-headphone accessories.

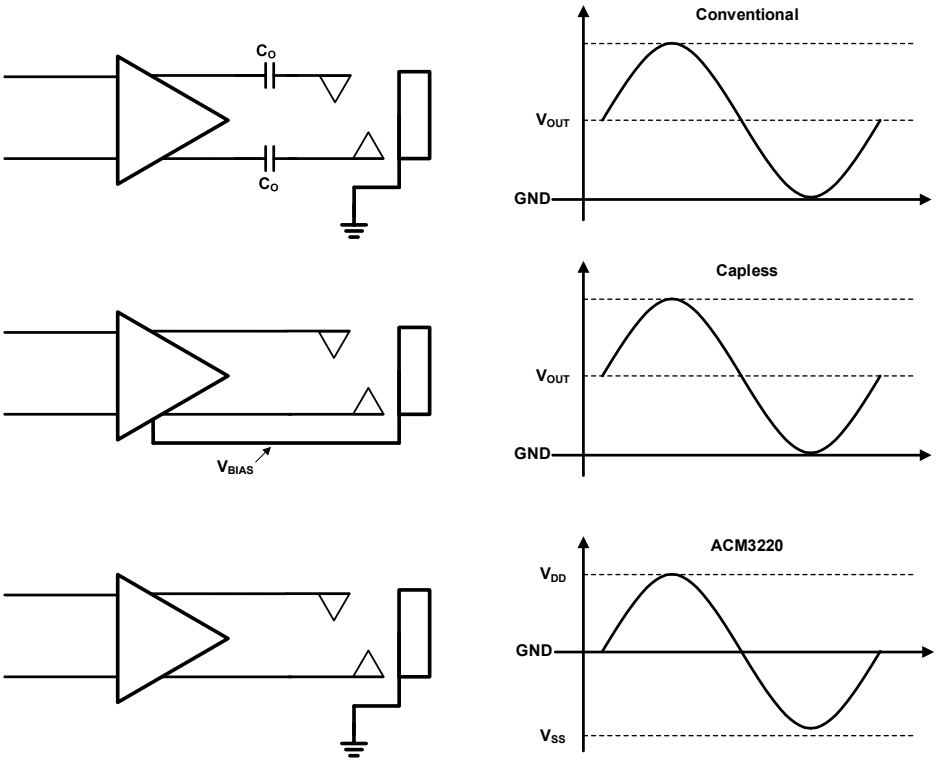


Figure 18 Amplifier Applications

9.3.2 Eliminating Turn-on Pop and Power Supply Sequencing

The ACM3220 has excellent noise and turn-on/turn-off pop performance. It uses and integrated click-and-pop suppression circuit to allow fast start-up and shutdown without generating any voltage transients at the output pins. Typical start-up time from shutdown is 5ms.

ACM3220 keeps the output DC voltage at 0V even when the amplifier is powered up. The active pop-and-click suppression circuit eliminates audible transients during start up and shutdown.

Use input coupling capacitors to ensure inaudible turn-on pop. Activate the ACM3220 after all audio sources have

been activated and their output voltages have settled. On power-down, deactivate the ACM3220 before deactivating the audio input source. The EN pin controls device shutdown: Set to 0.6V or lower to deactivate the ACM3220; set to 1.3V or higher to activate.

9.3.2 RF and Power Supply Immunity

The ACM3220 employs a new differential amplifier architecture to achieve high power supply noise rejection and RF noise rejection. RF and power supply noise are common in modern electronics. Although RF frequencies are much higher than the 20kHz audio band, signal modulation often falls in-band. This, in turn, modulates the supply voltage, allowing a coupling path to the audio amplifier. A common example is the 217Hz GSM frame-rate buzz often heard from an active speaker when a cell phone is placed nearby during a phone call.
The ACM3220 has excellent rejection of power supply and RF noise, preventing audio signal degradation.

9.3.4 Constant Maximum Output Power and Acoustic Shock Prevention

Typically the output power increases with increasing supply voltage on an unregulated headphone amplifier. The ACM3220 maintains a constant output power independent of the supply voltage. Thus the design for prevention of acoustic shock (hearing damage due to exposure to a loud sound) is simplified since the output power will remain constant, independent of the supply voltage. This feature allows maximizing the audio signal at the lowest supply voltage.

9.3.5 Gain Control

The ACM3220 has four gain settings which are controlled with pin G0 and G1. Table 1 gives an overview of the gain function.

Table 1 Gain Setting

G0 Voltage	G1 Voltage	AMPLIFIER GAIN
≤ 0.5V	≤ 0.5V	-6 dB
≥ 1.3V	≤ 0.5V	0 dB
≤ 0.5V	≥ 1.3V	3 dB
≥ 1.3V	≥ 1.3V	6 dB

9.4 Application and Implementation

9.4.1 Application Information

The ACM3220 starts its operation by asserting the EN pin to logic 1. The device enters in shutdown mode when pulling low EN pin. The charge pump generates a negative supply voltage. The charge pump flying capacitor connected between CPP and CPN transfers charge to generate the negative supply voltage. The output voltage are capable of positive and negative voltage swings and are centered close to 0V, eliminating the need for output capacitors. Input coupling capacitors block any DC bias from the audio source and ensure maximum dynamic range. The device has built-in pop suppression circuitry to completely eliminate pop noise during turn-on, turn-off and enter or exit shutdown mode.

9.4.2 Typical Applications-Configuration with Differential Input Signals

Figure 17 shows a typical application circuit for the ACM3220 with a stereo headphone jack output and differential input signals. Also supports charge pump flying capacitor and power supply decoupling capacitors.

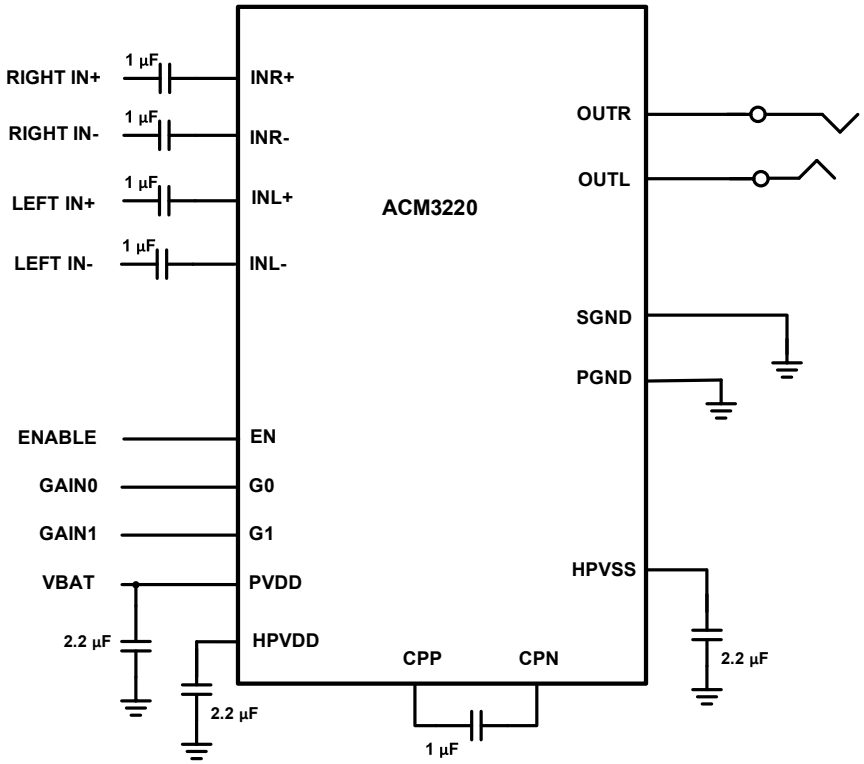


Figure 17 Typical Application Configuration with Differential Input Signals

9.4.2.1 Design Requirements

For this design example, use the parameters shown in Table 2.

Table 2. Design Parameters

PARAMETERS	VALUES
Input Voltage Range	2.5V-5.5
Output Voltage	1.1 Vrms

9.4.2.2 Detailed Design Procedure

9.4.2.2.1 Input Coupling Capacitors

Input coupling capacitors block any DC bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize ACM3220 turn-on pop to an inaudible level.

The input capacitors are in series with ACM3220 internal input resistors, creating a high-pass filter. Equaltion 3 calculates the high-pass filter corner frequency. The input impedance, RIN, is dependent on device gain. Larger input capacitors decrease the corner frequency. See the Operating Characteristics table for input impedance values.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} \quad (3)$$

For a given high-pass cutoff frequency, the minimum input coupling capacitor is found as:

$$C_{IN} = \frac{1}{2\pi R_{IN} f_C} \quad (4)$$

Example: Design for a 20Hz corner frequency with a ACM3220 gain of +6 dB. The Operating Characteristics table gives RIN as 13.2kΩ. Equation 4 shows the input coupling capacitors must be at least 0.6μF to achieve a 20 Hz high-pass corner frequency. Choose a 0.68μF standard value capacitor for each ACM3220 input (X5R material or better is required for best performance, prefer X7R material).

9.4.2.2.2 Charge Pump Flying Capacitor and HPVSS Capacitor

The ACM3220 uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CPP and CPN. It transfers charge to generate the negative supply voltage. The HPVSS capacitor must be at least equal in value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance) to maximize charge pump efficiency. Typical values are 1μF to 2.2μF for the HPVSS and flying capacitors. Although values down to 0.47μF can be used, total harmonic distortion (THD) will increase.

9.4.3 Typical Applications-Configuration with Single-Ended Input Signals

Figure 18 shows a typical application circuit for the ACM3220 with a stereo headphone jack output and single-ended input signals. Also supports charge pump flying capacitor and power supply decoupling capacitors.

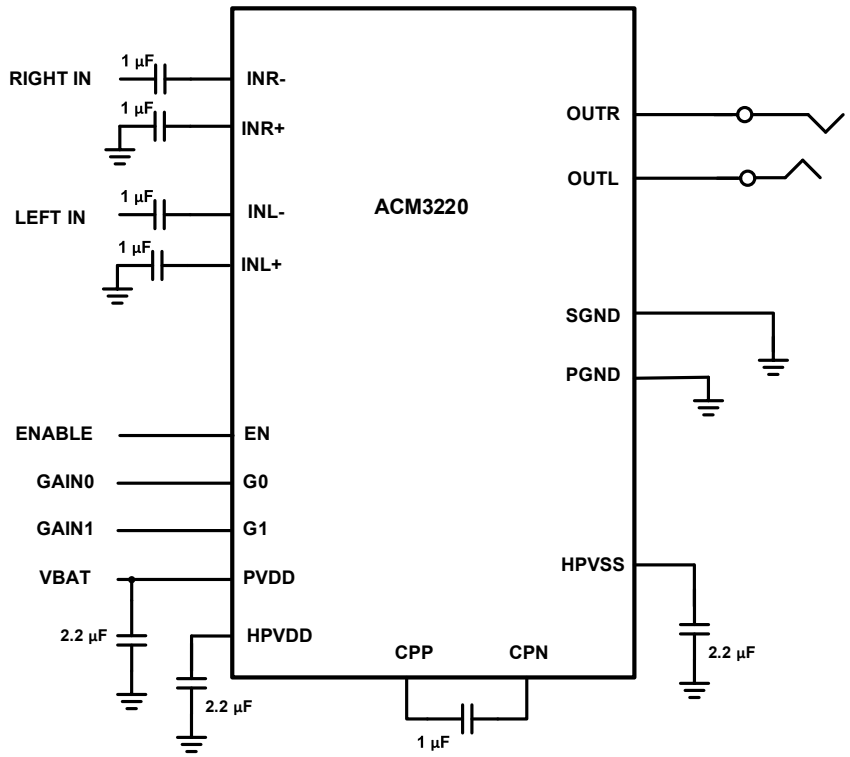


Figure 18 Typical Application Configuration with Single-Ended Input Signals

9.5 Power Supply Recommendations

Connect the supply voltage to the VDD pin and decouple it with X5R or better capacitor. Connect the HPVDD pin only to a 2.2μF, X5R or better, capacitor. Do not connect HPVDD to an external voltage supply. Place both capacitors with 5mm of their associated pins on the ACM3220. Ensure that the ground connection of each of the capacitors has a minimum length path to the device. Failure to properly decouple the ACM3220 may degrade audio for EMC performance.

9.5.1 Power Supply and HPVDD Decoupling Capacitors

The ACM3220 headphone amplifiers requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance). Place a 2.2μF capacitor within 5mm of the VDD pin. Reducing the distance between the decoupling capacitor and VDD minimizes parasitic inductance and resistance, improving ACM3220 supply rejection performance. Use 0402 or smaller size capacitor if possible.

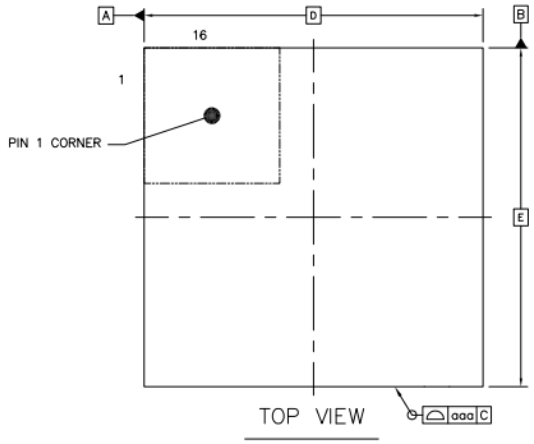
For additional supply rejection, connect an additional 10μF or higher value capacitor between VDD and ground. This will help filter lower frequency power supply noise. The high power supply rejection ratio (PSRR) of the ACM3220 makes the 10μF capacitor unnecessary in most applications.

Connect a 2.2μF capacitor between HPVDD and ground. This ensures the amplifier internal bias supply remains stable and maximizes headphone amplifier performance.

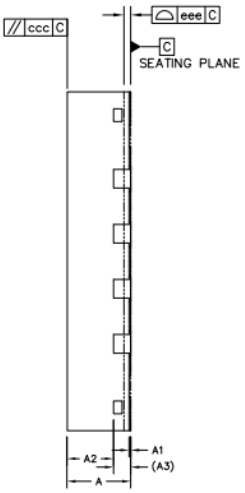
Please note that: Do not connect HPVDD directly to VDD or an external supply voltage. The voltage at HPVDD is generated internally. Connecting HPVDD to an external voltage can damage the device.

10. Package Dimensions

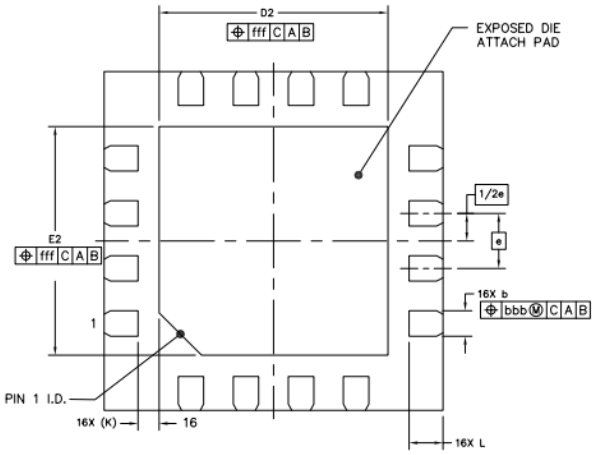
Orderable Device	Package Type	MPQ	MOQ	Eco Plan	MSL Level	Device Marking
ACM3220	QFN Tape and Reel	3000	3000	RoHS Compliant Lead-Free Finish	MSL3	ACM3220



TOP VIEW



SIDE VIEW



BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.25	0.3	0.35
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.65 BSC	
EP SIZE	X	D2	2.6	2.7	2.8
	Y	E2	2.6	2.7	2.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	