2×25W 立体声 | 1×50W 单声道，I2S，D 类音频放大器，集成音频算法

1. 描述

CCD6805S 是一款高集成、高效率、数字输入的 D 类立体声音频放大器，创新使用多项节能模式减小芯片过热，内置 DSP，提供多种音效算法，能够提供 2×25W 的立体声输出或 1×50W 的单声道输出。

CCD6805S 内置保护电路，可提供过流保护、过温保护、直流偏移保护、欠压保护和过压保护以及时钟错误保护。CCD6805S 采用 I2S/TDM 音频接口， 具备丰富的音频处理模块，包括音量控制（Vol）、可编程均衡器（EQ）、3 段式动态范围增益控制（DRC）、自动增益控制（AGL）、动态 Biquad（DPEQ）、虚拟声场（Spatializer）以及高达 4.5ms 的预测式 DRC，提前观测信号变化，实现平滑的音效控制。

CCD6805S 集成了先进的扩频技术，以抑制系统电磁干扰（EMI）。可以选择使用铁氧体磁珠滤波器来替代的电感，从而减少电路板空间和成本。

2. 特性与优点

- 输出功率：

BTL, <1% THD Power 持续功率，推荐 **384KHz + HE** **(**室温开始 **1KHz** 持续 **1** 分钟, 另 **Peak** 功率持续 **2** 秒**)**				
	12V	13.5V	18V	24V
4Ω	15W	19W	34W(peak) 20W	N/A
6Ω	11W	14W	25W	44W(peak) 30W
8Ω	8.5W	10.5W	19.5W	34W
10Ω	7W	9W	16W	28W
PBTL, <1% THD Power 持续功率，推荐 **384KHz + HE** **(**室温开始 **1KHz** 持续 **1** 分钟, 另 **Peak** 功率持续 **2** 秒**)**				
2Ω	30W	38W	67W(peak) 40W	N/A
3Ω	22W	28W	50W	88W(peak) 60W
4Ω	16W	20W	38W	65W

- 供电电压范围：
  - PVDD: 4.5V 至 26.4V
  - DVDD: 1.8V 或 3.3V
  - AVDD: 5V 外供（直供节能模式）或片上自偏置产生
- 多项创新节能模式:
  - 直供节能模式 （Direct ECO mode）：AVDD pin 外部 5V 供电，显著降低芯片待机发热
  - 智感静默模式 （Smart Silent mode）：该模式下无音乐信号输入时，通道自动进入休眠，有音乐信号无延时快速恢复
- 音频性能指标
  - Noise: < 5uVrms Smart Silent enable
  - THD+N ≤ 0.02% at 1W, 1kHz
  - SNR ≥ 108dB (A-weighted)
  - PVDD idle current in play mode < 1mA
- 音频输入信号格式
  - 3-wire I2S, LJ, RJ, TDM
  - Fs 支持 44.1/48KHz, 88.2kHz/96KHz
  - 支持独立回声消除通道 SDOUT
- 音频 DSP 算法
  - 2 × 15 EQs + 3-band DRC + AGL + 3 × post EQs
  - Sub-woofer channel： 5 × EQs + 1 × DRC + 2 × post EQs
  - 动态 EQ（DPEQ）
  - 虚拟声场（Spatializer）
  - 支持 Class-H
  - 预测式 DRC
- 保护功能
  - 过流/过压/过温/欠压/直流保护
  - 支持自发热管理调节（TFB）
- 调音及系统集成
  - 一站式 GUI 调音软件
  - 支持上位机一键生成配置文件

3. 应用

- AI 音箱，蓝牙音箱，条形音箱
- 电视，笔记本，平板，智能家居
- 家庭影院，会议系统

器件信息

器件编号	封装	封装尺寸（标称值）
CCD6805S	TSSOP28-EP 散热片朝下	9.7 mm × 4.4 mm

选型表

Device Name	Power	Input	Rdson	1% THD Output Power	DSP	Class H	Feature
CCA3136	3.5V-14.5V	Analog	120	2x10W@12v,6ohm	N	N	低噪声，动态好
CCA3110	3.5V~14.5V	Analog	120	2x10W@12v,6ohm	N	N	低噪声，动态好
CCD6805S	4.5~26V	I2S/TDM	110	2x25w@18v,6ohm	Y	Y	15Eq, 3-DRC, ClassH, Spatializer AVDD 直供节能, 智感静默
CCD6805L	4.5~21V	I2S/TDM	110	2x25W@21V,6ohm	Y	Y	15Eq, 3-DRC, ClassH, Spatializer AVDD 直供节能, 智感静默
CCD6805	4.5~21V	I2S/TDM	110	2x25W@21V,6ohm	Y	Y	15Eq, 3-DRC, ClassH, Spatializer AVDD 直供节能, 智感静默
CCA3118	4.5~26V	Analog	65	2x30w@24v,8ohm	N	N	低噪声，动态好
CCD6825	4.5~26V	I2S/TDM	65	2x38w@24v,8ohm	Y	Y	15Eq, 3-DRC, ClassH, Spatializer AVDD 直供节能, 智感静默
CCD6827	4.5~26V	I2S/TDM	65	2x47w@25v,6ohm	Y	Y	15Eq, 3-DRC, ClassH, Spatializer AVDD 直供节能, 智感静默
CCD6828	4.5~26V	I2S/TDM	65	2x50w@23v,4ohm	Y	Y	15Eq, 3-DRC, ClassH, Spatializer AVDD 直供节能, 智感静默
CCA3116	4.5~26V	Analog	65	2x50w@23v,4ohm	N	N	低噪声，动态好
CCD12071	4.5V~26V	I2S/TDM	60	1x60W@24v,4ohm	N	N	实时温度，实时电压
CCD12079	5.5V~25V	I2S/TDM	60	4x65w@25v,4ohm	N	N	数字分频, HiRes，实时温度，实时电压
CCD12076	4.5~26V	I2S/TDM	60	4x65w@25v,4ohm	N	N	实时温度，实时电压, 4 通道, 2.1, 2.0 模式
CCD6830	4.5~32V	I2S/TDM	65	2x75w@32v,6ohm	Y	Y	15Eq, 3-DRC, ClassH, Spatializer AVDD 直供节能, 智感静默
CLD6255	4.5~42V	I2S/TDM	55	4x200w@42v,4ohm	N	Y	超大功率，实时温度，实时电压，低延时

目录

4. 引脚配置与功能

图 **4-1** **Tssop28-ep pad down，top view**

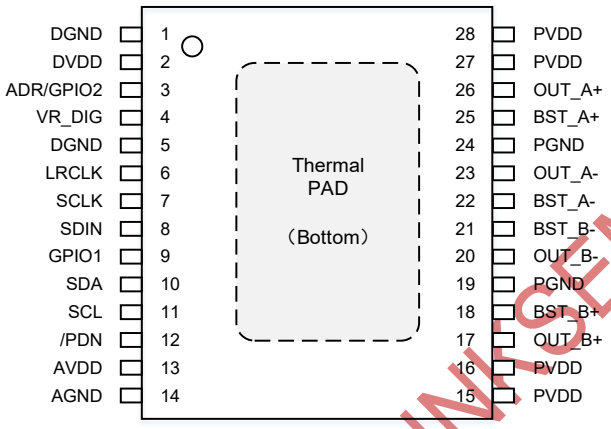

表 **4-1** 引脚功能

引脚		描述
名称	编号	
DGND	1	数字地
DVDD	2	3.3-V 或 1.8-V 数字电源
VR_DIG	4	内部调节的 1.8V 数字供电电压。该引脚不得用于驱动外部设备。
ADR/GPIO2	3	通过不同的上拉电阻连接到 DVDD，可以设置不同的 I2C 设备地址。在上电后，ADR 引脚可以重新定义为 GPIO 功能。
DGND	5	数字地
LRCLK	6	串行端口输入数据线上激活的数字信号的字选择时钟。在 I2S、左对齐（LJ）和右对齐（RJ）模式下，这对应于左声道和右声道的边界。在 TDM 模式下，对应帧同步信号。
SCLK	7	I2S/TDM 串行时钟
SDIN	8	I2S/TDM 串行数据
GPIO1	9	通用输入/输出
SDA	10	I2C 串行控制数据接口输入/输出
SCL	11	I2C 串行控制时钟输入
/PDN	12	关断控制，低电平有效。/PDN 将放大器置于关机状态，关闭所有内部稳压器, I2C 不能通信。 低电平：关闭设备；高电平：启用设备。
AVDD	13	传统模式： AVDD 由内部 LDO 产生，外接 Bypass 电容产生偏置电压，无需外部电源。 直供节能模式（Direct ECO Mode）：AVDD 外部供电 4.85V-5.3V，此模式可以降低 PVDD 上的静态功耗，显著降低芯片待机时的功耗。
AGND	14	模拟地
PVDD	15,16,27,28	功率级电源
PGND	19,24	为功率器件电路提供接地参考。将此引脚连接到系统地。
OUT_A+	26	差分扬声器放大器输出的正端子 A+ （左通道或 CH1+）
BST_A+	25	OUT_A+ 引脚的自举电容连接点，该电容用于为 OUT_A+ 的高边栅极驱动提供电源。

OUT_A-	23	差分扬声器放大器输出的负端子 A-（左通道或 CH1-）
BST_A-	22	OUT_A- 引脚的自举电容连接点，该电容用于为 OUT_A- 的高边栅极驱动提供电源。
BST_B-	21	OUT_B- 引脚的自举电容连接点，该电容用于为 OUT_B- 的高边栅极驱动提供电源。
OUT_B-	20	差分扬声器放大器输出的负端子 B- （右通道或 CH2-）
BST_B+	18	OUT_B+ 引脚的自举电容连接点，该电容用于为 OUT_B+ 的高边栅极驱动提供电源。
OUT_B+	17	差分扬声器放大器输出的正端子 B+（右通道或 CH2+）
PowerPAD™		连接到地

5. 绝对最大额定值

在自由空气操作温度范围内（除非另有说明），请参阅 (1)

		最小值	最大值	单位
电压	低压数字供电，DVDD	-0.3	3.9	V
	PVDD 供电，PVDD	-0.3	32	
	以 DVDD 为参考的数字输入 (2)，输入电压 $V_{I(DigIn)}$	-0.3	VDVDD+0.5	
	AVDD pin, 外部供电直供节能模式	-0.3	5.5	
	扬声器输出引脚上的电压，$V_{I(SPK\_OUTxx)}$	-0.3	32	
电阻	负载电阻，R_L	2.4		Ω
温度	环境工作条件，T_A	-25	85	°C
	结温，T_J	-40	180	
	存储条件，T_{stg}	-40	125	

(1) 超出绝对最大额定值范围运行可能导致设备永久损坏。绝对最大额定值并不意味着设备在这些条件或超出推荐工作条件所列的任何其他条件下能够正常运行。如果在推荐工作条件之外，但仍在绝对最大额定值范围内使用，设备可能无法完全正常工作，这可能会影响设备的可靠性、功能、性能，并缩短设备的使用寿命。

(2) 以 DVDD 为参考的数字引脚包括：ADR/GPIO2、LRCLK、SCLK、SCL、SDA、SDIN 和 /PDN。

6. 推荐工作条件

			最小值	典型值	最大值	单位
PVDD	电源供电输入		4.5		26.4	V
DVDD	电源供电输入		1.65		3.63	V
R_{SPK}	最小扬声器负载	4.5-18V		4		Ω
R_{SPK}	最小扬声器负载 (3)	18-26.4V	5.5	8		Ω
L_{OUT}	短路条件下 LC 滤波器中的最小电感值		1	4.7		μH
T_J	结温		-40		150	°C

(3) 最小扬声器负载由过流保护（OCE）阈值限制。如果输出峰值电流小于 6.5A，CCD6805S 还支持在高 PVDD 电压下使用更低的扬声器负载。对于 BTL 模式，过流保护阈值为 6.5A（典型值）；对于 PBTL 模式，过流保护阈值为 13A（典型值）。最小扬声器负载取决于输出峰值电压。

7. 静电等级

			值	单位
$V_{(ESD)}$	静电放电	人体模型（HBM），符合 ANSI/ESDA JEDEC JS-001 标准，所有引脚 (4)	±4000	V
		充电器件模型（CDM），符合 JEDEC 标准 JESD22-C101，所有引脚 (5)	±500	

(4) JEDEC 文件 JEP155 指出，500V 人体模型（HBM）允许在标准静电防护控制流程下安全进行生产制造。

(5) JEDEC 文件 JEP157 指出，250V 充电器件模型（CDM）允许在标准静电防护控制流程下安全进行生产制造

8. 热信息

热性能指标		CCD6805S TSSOP (28) 28 PINS	单位
$R_{\theta JA}$	结到环境的热阻	30	°C/W
$R_{\theta JB}$	结到基板的热阻	11	°C/W
Ψ_{JT}	结到顶部的特性参数	0.3	°C/W
Ψ_{JB}	结到基板的特性参数	11	°C/W
$R_{\theta JC(top)}$	结到外壳（顶部）的热阻	13	°C/W
$R_{\theta JC(bot)}$	结到外壳（底部）的热阻。	2	°C/W

9. 时序要求

音频接口时序		最小值	典型值	最大值	单位
Fsclk	SCLK (bit clock) frequency			24.576	MHz
Tsclk	SCLK period	41			ns
Tsclk_duty	SCLK duty cycle	45	50	55	%
Tsclkh	SCLK high time	16			ns
Tsclkl	SCLK low time	16			ns
Tds	SDIN setup time before SCLK rising edge	8			ns
Tdh	SDIN hold time after SCLK rising edge	8			ns
Trise/fall	SCLK rising and fall time			5	ns
Tfsynch	FSYNC high time	1 Tsclk			ns
Tfsyncs	FSYNC setup time	8			ns
Tfsynchd	FSYNC hold time	8			ns
Ci	Input capacitance, SLCK, FSYNC, SDIN1, SDIN2			10	pf

10. 电气特性

下表列出了 CCD6805S 的电气特性（默认测试条件 384k HE Mode，除非另有说明）：

参数		测试条件	最小值	典型值	最大值	单位
$A_{V(SPK\_AMP)}$	可编程增益	该值表示“峰值电压”，不考虑由于较低的 PVDD 导致的削波。在 0dB 输入（1FS）时测量	4.95		29.5	V
$\triangle A_{V(SPK\_AMP)}$	放大器增益误差	增益=26Vp/Fs		0.5		dB
Shutdown current	PVDD 关断电流			4		μA
IPVDD	PVDD Idle 电流	HE MODE,12V，直供节能模式，		9		mA
		直供节能模式 + 智感静默模式		1		mA
		传统模式		21		mA
f_{SPK_AMP}	扬声器放大器的开关频率			384		kHz
				480		kHz
				576		kHz
				768		kHz
$R_{DS(on)}$	单个输出 MOSFET 的导通时漏极至源极电阻	场效应晶体管（FET）+ 金属化层		110		mΩ
OCE_{THRES}	过流错误阈值	OUTxx 过流错误阈值	6	7.5		A
$OCE_{THRES（PVDD）}$	PVDD 过压错误阈值			28		V
$UVE_{THRES（PVDD）}$	PVDD 欠压错误阈值			4		V
OTE_{THRES}	过温错误阈值			160		°C
$OTE_{Hystersis}$	过温错误回差			10		°C
OTW_{THRES1}	过温预警等级 1	寄存器读 0x73 bit3		146		°C
OTW_{THRES2}	过温预警等级 2	寄存器读 0x73 bit2		135		°C
扬声器放大器（立体声桥接负载，**BTL**）						
|VOS|	放大器偏移电压	在零输入数据下以差分方式测量，增益配置为 29.5Vp，VPVDD = 12V，HE 模式，关闭智感静默模式	-5		5	mV
		在零输入数据下以差分方式测量，增益配置为 29.5Vp，VPVDD = 12V，HE 模式，打开智感静默模式	-1		1	
PO(SPK)	单通道输出功率	VPVDD = 21V, SPK_GAIN = 24.8 Vp/FS, RSPK = 8 Ω, f = 1 kHz, THD+N = 1%, HE Mode		25		W
		VPVDD = 21V, SPK_GAIN = 24.8 Vp/FS, RSPK = 8 Ω, f = 1 kHz, THD+N = 10%, HE Mode		32		
		VPVDD = 18 V, SPK_GAIN = 20.8 Vp/FS, RSPK = 6 Ω, f = 1 kHz, THD+N = 1%, BD Mode		24		
		VPVDD = 18 V, SPK_GAIN = 20.8 Vp/FS, RSPK = 6 Ω, f = 1 kHz, THD+N = 10%, BD Mode		30		
		VPVDD = 12 V, SPK_GAIN = 13.9 Vp/FS, RSPK = 6 Ω, f = 1 kHz THD+N = 1%, BD Mode		10		
		VPVDD = 12 V, SPK_GAIN = 13.9 Vp/FS, RSPK = 6 Ω, f = 1 kHz THD+N = 10%, BD		13		

		Mode				
		VPVDD = 13.5 V, SPK_GAIN = 15.6 Vp/FS, RSPK = 6 Ω, f = 1 kHz THD+N = 1%, BD Mode		13		
		VPVDD = 13.5 V, SPK_GAIN = 15.6 Vp/FS, RSPK = 6 Ω, f = 1 kHz THD+N = 10%, BD Mode		17		
		VPVDD = 24 V, SPK_GAIN = 28 Vp/FS, RSPK = 6 Ω, f = 1 kHz, THD+N = 1%, HE Mode		42		
		VPVDD = 24 V, SPK_GAIN = 28 Vp/FS, RSPK = 6 Ω, f = 1 kHz, THD+N = 10%, HE Mode		53		
$THD+N_{SPK}$	总谐波失真加噪声 (P_O = 1W, f = 1kHz, R_{SPK} = 6Ω)	V_{PVDD} = 12V, FSW = 768kHz, SPK_GAIN = 13.9Vp/FS, LC-filter, BD mode		0.02		%
		V_{PVDD} = 18V, FSW = 768kHz, SPK_GAIN = 20.8Vp/FS, LC-filter, BD mode		0.02		
$I_{CN(SPK)}$	0 数据输入时候，芯片 play 状态下噪声	VPVDD = 12V, LC-filter, load = 6Ω, Smart Silent disable		40		μV_{RMS}
		VPVDD = 24V, LC-filter, load = 6Ω, Smart Silent disable		40		
		VPVDD = 12V, LC-filter, load = 6Ω, Smart Silent enable			5	
		VPVDD = 24V, LC-filter, load = 6Ω, Smart Silent enable			5	
Efficiency	PVDD 效率	12V, 4Ω, HE mode, 2x20W		93		%
		12V, 4Ω, HE mode, 2x1W, Direct Power Supply Efficiency Mode enable		88		%
		12V, 4Ω, HE mode, 2x1W, Direct Power Supply Efficiency Mode disable		84		%
DR	动态范围	A-Weighted, –60dBFS method. PVDD = 24V, SPK_GAIN = 29.5Vp/FS		110		dB
SNR	信噪比	A-Weighted, referenced to 1% THD+N output level, PVDD = 24V		112		dB
K_{SVR}	电源抑制比	Injected noise = 1kHz, 1VRMS, PVDD = 13.5V, input audio signal = digital zero		72		dB
$X\text{-}talk_{SPK}$	串扰（最坏情况下左声道到右声道以及右声道到左声道的耦合）	f = 1 kHz		95		dB
扬声器放大器（单通道，**PBTL**）						
$THD+N_{SPK}$	总谐波失真加噪声 (P_O = 1W, f = 1kHz)	VPVDD = 18 V, LC-filter, RSPK = 2 Ω		0.055		%
		VPVDD = 24 V, LC-filter, RSPK = 3 Ω		0.035		
PO	单通道输出功率	VPVDD = 18 V, SPK_GAIN = 20.8 Vp/FS, RSPK = 3 Ω, f = 1 kHz, THD+N = 1%, HE Mode		47		W
		VPVDD = 18 V, SPK_GAIN = 20.8 Vp/FS, RSPK = 3 Ω, f = 1 kHz, THD+N = 10%, HE Mode		59		
		VPVDD = 24 V, SPK_GAIN = 28 Vp/FS, RSPK = 3 Ω, f = 1 kHz, THD+N = 1%, HE Mode		84		
		VPVDD = 24 V, SPK_GAIN = 28 Vp/FS, RSPK = 3 Ω, f = 1 kHz, THD+N = 10%, HE Mode		105		
SNR	信噪比	A-weighted, referenced to 1% THD+N output level, PVDD = 24V, RSPK = 4 Ω		110		dB
K_{SVR}	电源抑制比	Injected noise = 1kHz, $1V_{RMS}$, PVDD= 12V, input audio signal = digital zero		72		dB

11. 主要电气参数的典型曲线

所有测量均使用 CCD6805S 评估模块（EVM）测试 AP 滤波器设置 AES-17 20kHz。除非另有说明，所有测量均在音频频率设置为 1kHz 时进行。

BTL
384K

Figure 11-1 PVDD vs. Supply
PVDD=4-26V, BTL, HE

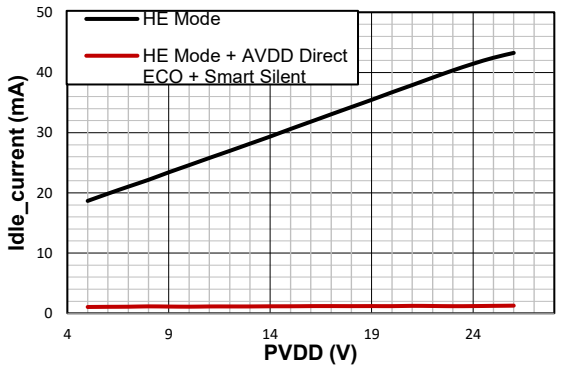

Figure 11-2 THD+N vs. Frequency
PVDD=12V, 4ohm, 1W, BTL, HE

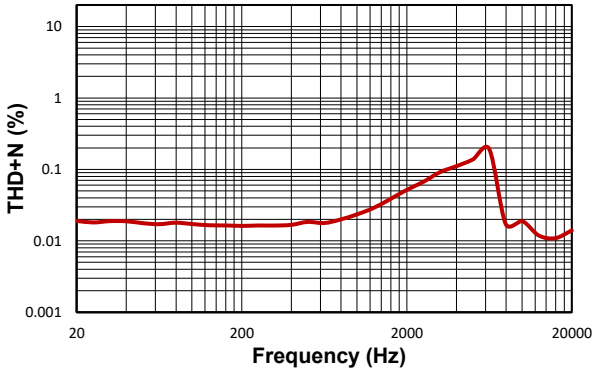

Figure 11-3 THD+N vs. Frequency
PVDD=12V, 8ohm, 1W, BTL, HE

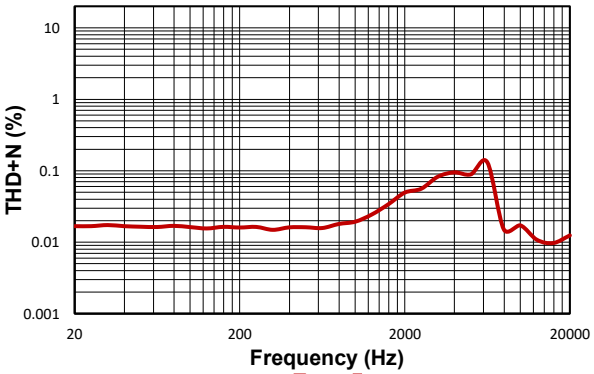

Figure 11-4 THD+N vs. Frequency
PVDD=18V, 6ohm, 1W, BTL, HE

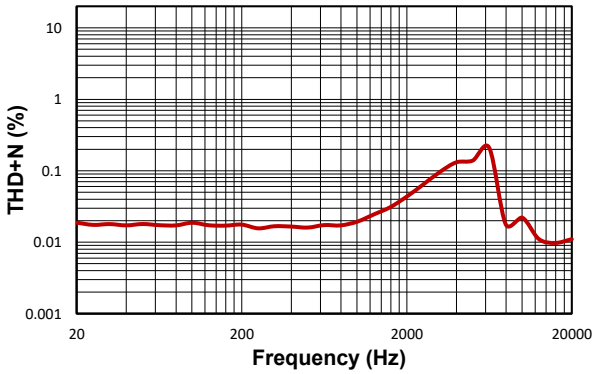

Figure 11-5 THD+N vs. Frequency
PVDD=24V, 6ohm, 1W, BTL, HE

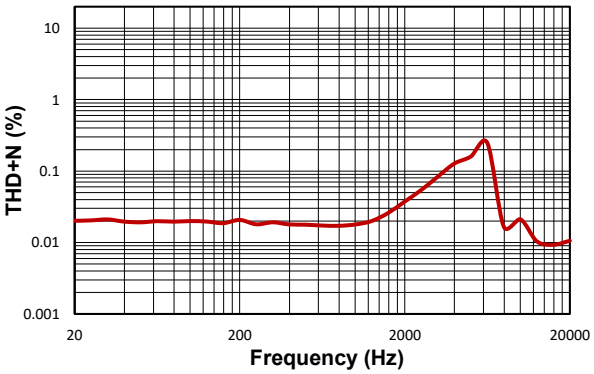

Figure 11-6 THD+N vs. Frequency
PVDD=24V, 8ohm, 1W, BTL, HE

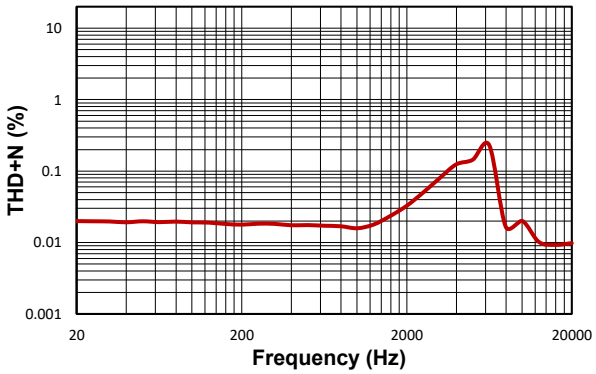

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Figure 11-7 Output Power vs. Supply Voltage
PVDD=6-18V, 4ohm, BTL，HE

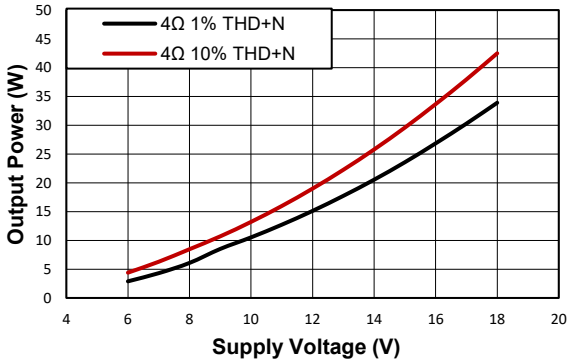

Figure 11-8 Output Power vs. Supply Voltage
PVDD=6-25V, 6ohm, BTL，HE

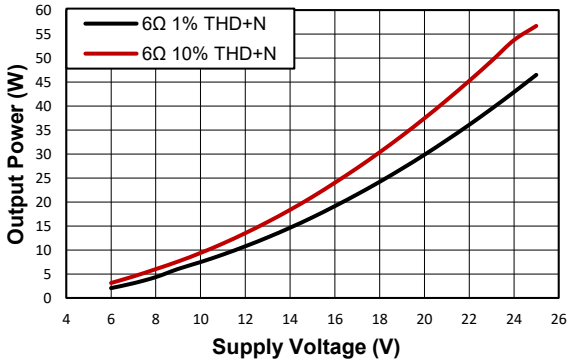

Figure 11-9 Output Power vs. Supply Voltage
PVDD=6-25V, 8ohm, BTL，HE

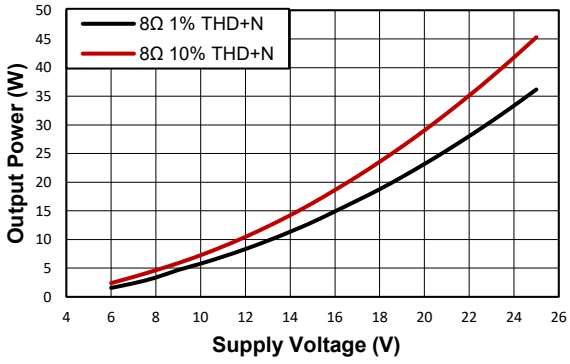

Figure 11-10 THD+N vs. Power
PVDD=12V, 4ohm, BTL, HE

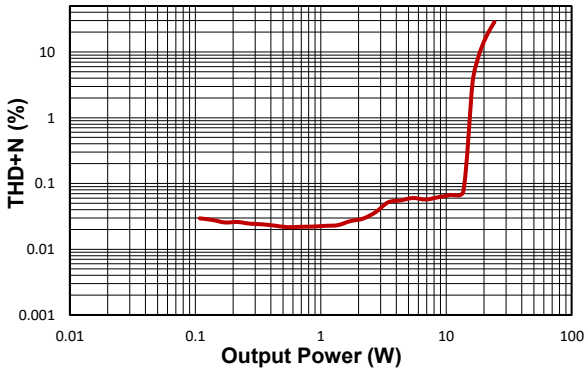

Figure 11-11 THD+N vs. Power
PVDD=12V, 8ohm, BTL, HE

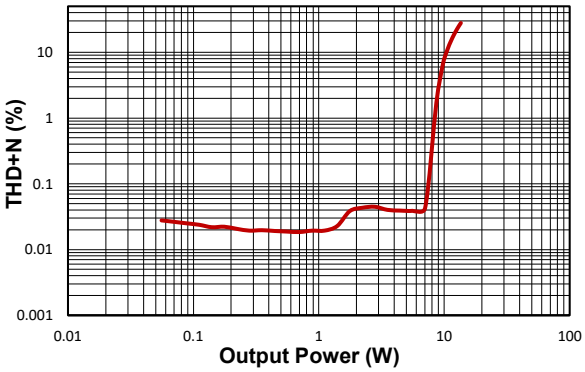

Figure 11-12 THD+N vs. Power
PVDD=18V, 6ohm, BTL, HE

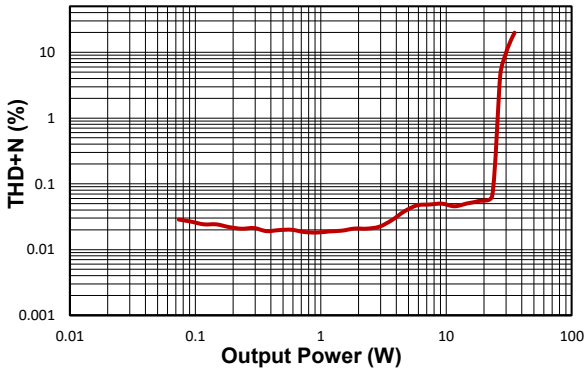

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Figure 11-13 THD+N vs. Power
PVDD=24V, 6ohm, BTL, HE

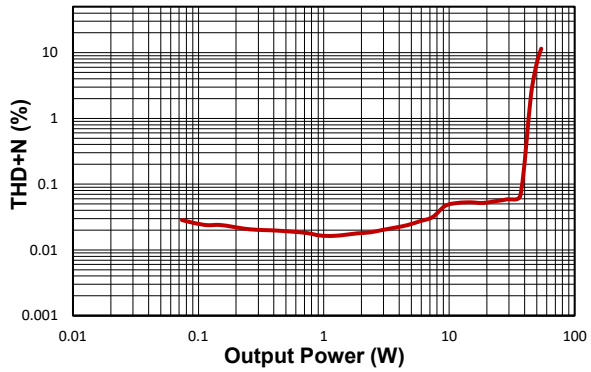

Figure 11-14 THD+N vs. Power
PVDD=24V, 8ohm, BTL, HE

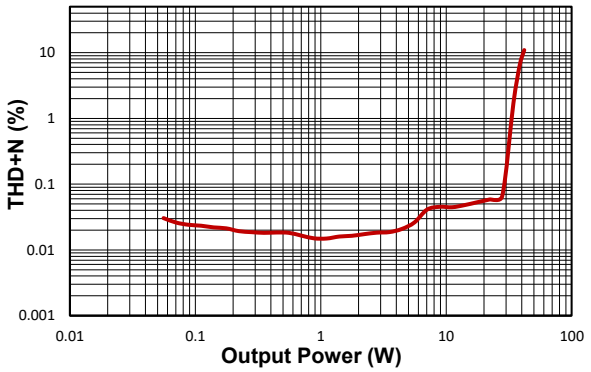

Figure 11-15 Efficiency vs. Output Power
PVDD=12V, 4ohm, BTL, HE

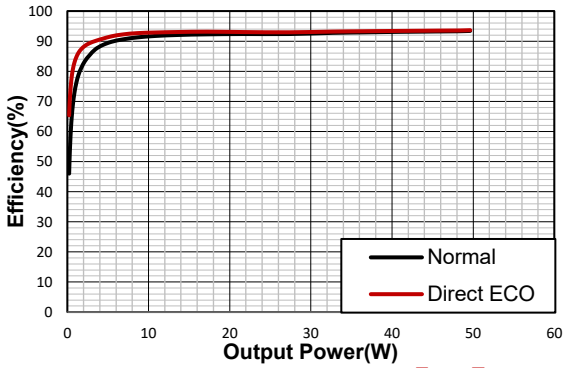

Figure 11-16 Efficiency vs. Output Power
PVDD=12V, 4ohm, BTL, HE

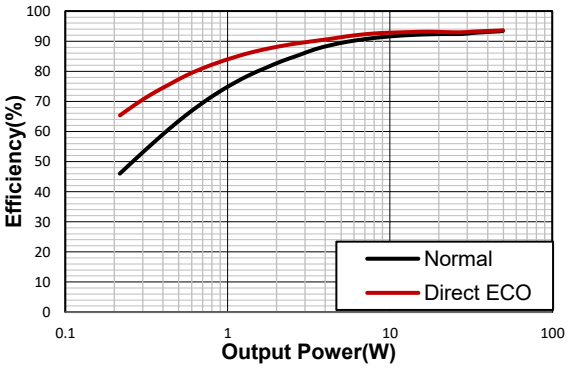

Figure 11-17 Power Loss vs. Output Power
PVDD=12V, 4ohm, BTL, HE

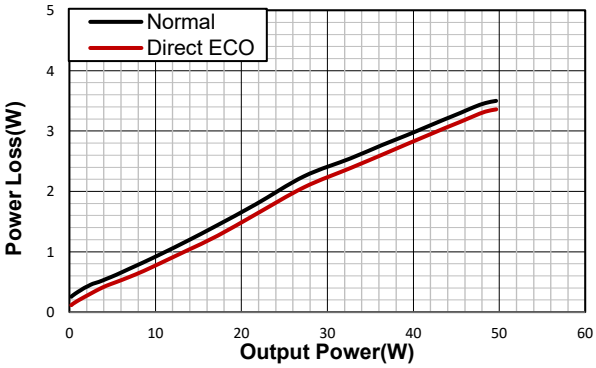

Figure 11-18 Efficiency vs. Output Power
PVDD=12V, 8ohm, BTL, HE

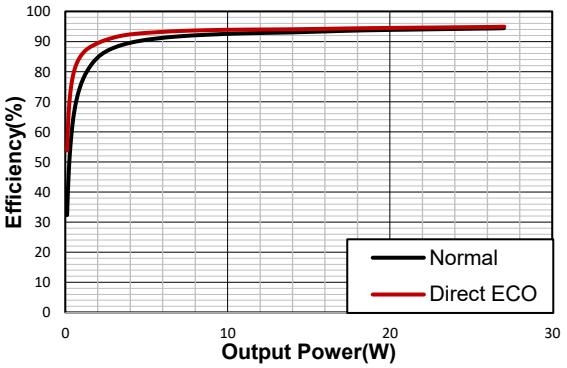

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Figure 11-19 Efficiency vs. Output Power
PVDD=12V, 8ohm, BTL, HE

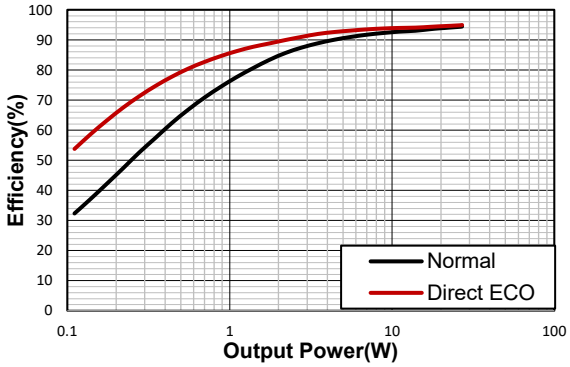

Figure 11-20 Power Loss vs. Output Power
PVDD=12V, 8ohm, BTL, HE

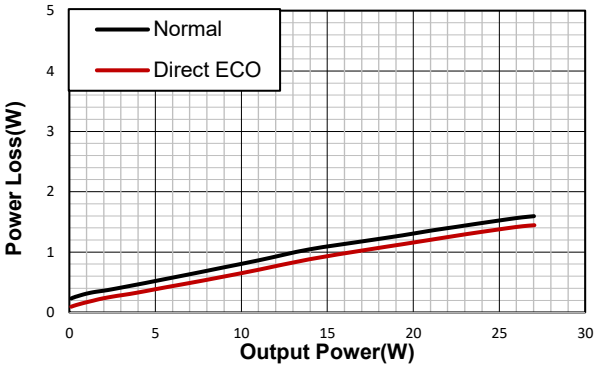

Figure 11-21 Efficiency vs. Output Power
PVDD=18V, 6ohm, BTL, HE

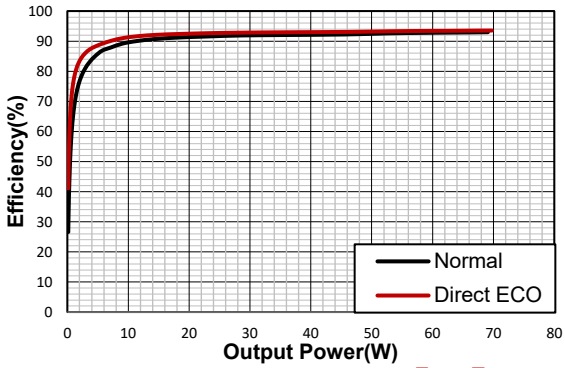

Figure 11-22 Efficiency vs. Output Power
PVDD=18V, 6ohm, BTL, HE

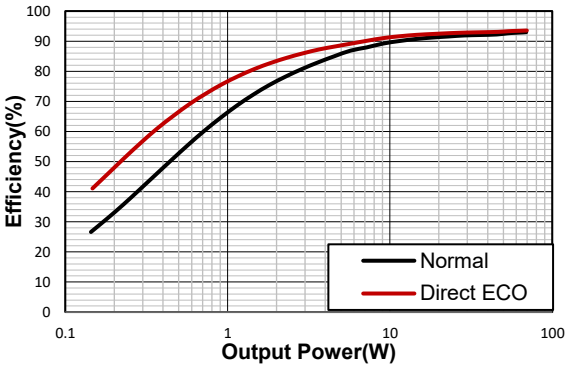

Figure 11-23 Power Loss vs. Output Power
PVDD=18V, 6ohm, BTL, HE

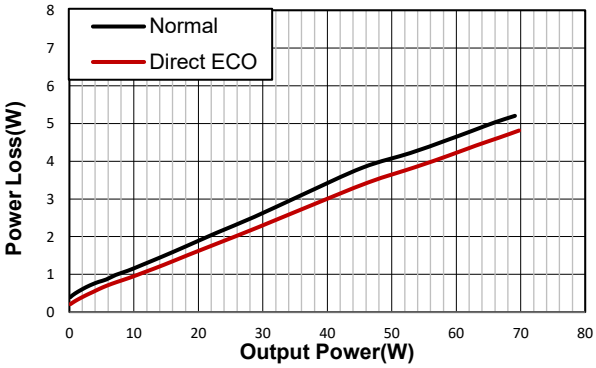

Figure 11-24 Efficiency vs. Output Power
PVDD=24V, 6ohm, BTL, HE

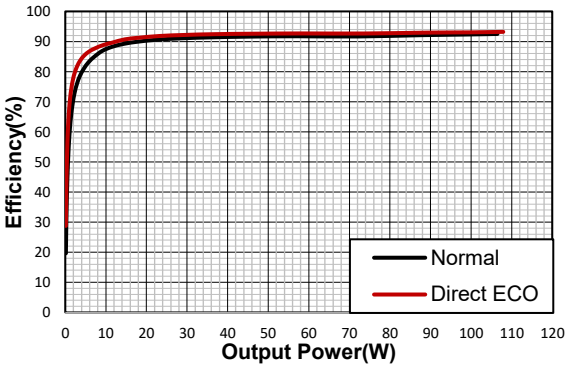

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Figure 11-25 Efficiency vs. Output Power
PVDD=24V, 6ohm, BTL, HE

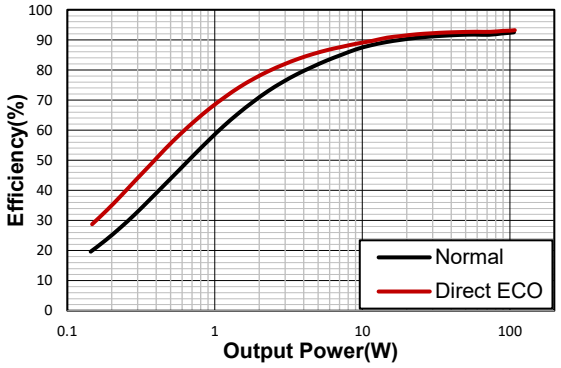

Figure 11-26 Power Loss vs. Output Power
PVDD=24V, 6ohm, BTL, HE

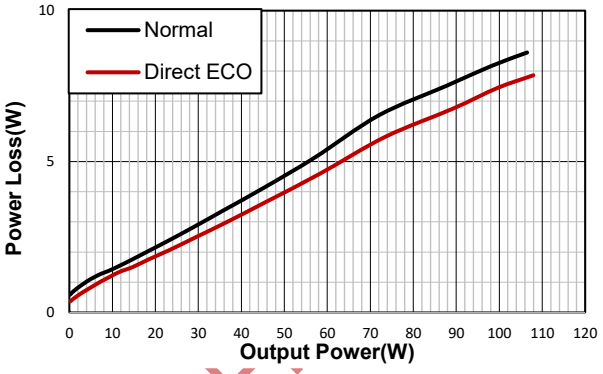

Figure 11-27 Efficiency vs. Output Power
PVDD=24V, 8ohm, BTL, HE

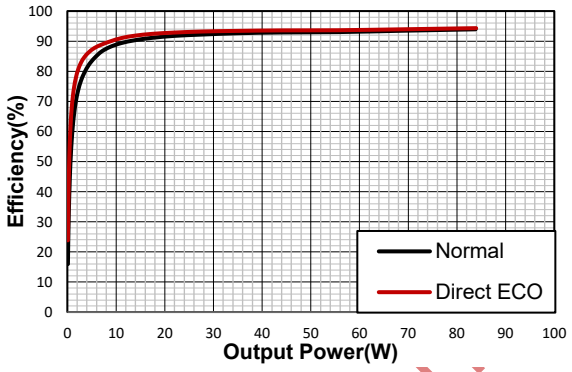

Figure 11-28 Efficiency vs. Output Power
PVDD=24V, 8ohm, BTL, HE

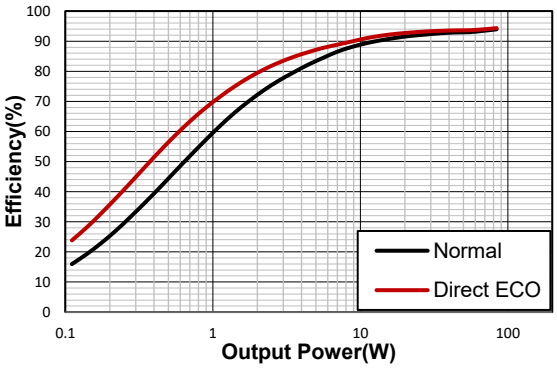

Figure 11-29 Power Loss vs. Output Power
PVDD=24V, 8ohm, BTL

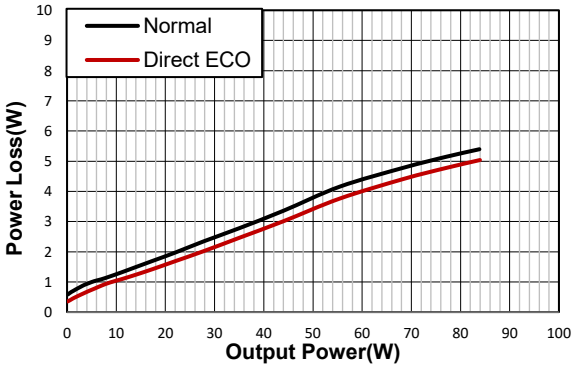

Figure 11-30 Crosstalk vs. Frequency
PVDD=12V, 4ohm, 1W, BTL, HE

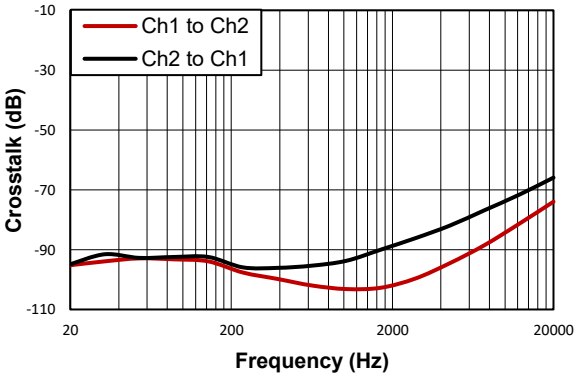

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Figure 11-31 Crosstalk vs. Frequency
PVDD=18V, 6ohm, 1W, BTL, HE

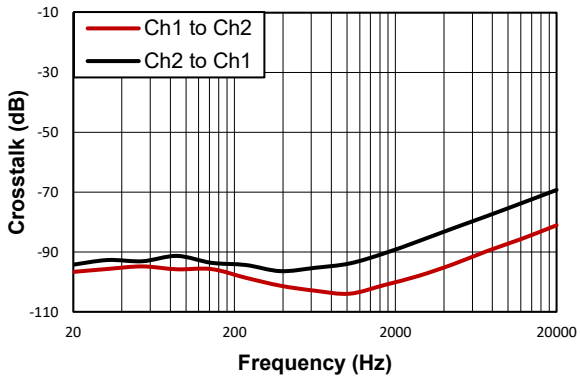

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Figure 11-32 THD+N vs. Frequency
PVDD=18V, 3ohm, 1W, PBTL, HE

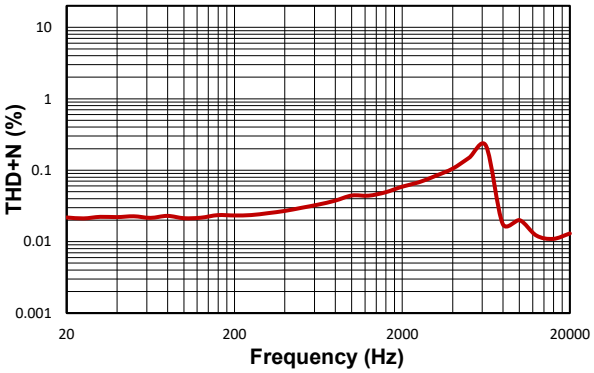

Figure 11-33 THD+N vs. Frequency
PVDD=24V, 3ohm 1W, PBTL, HE

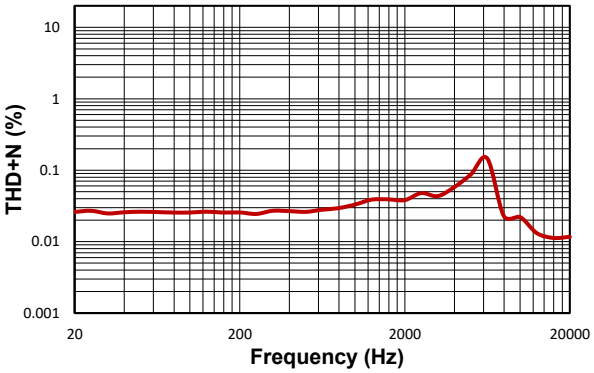

Figure 11-34 THD+N vs. Frequency
PVDD=24V, 4ohm, 1W, PBTL, HE

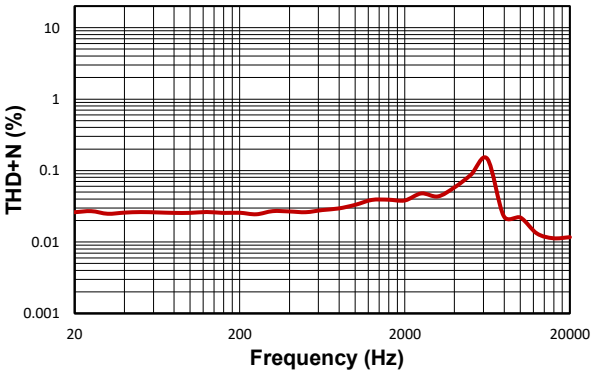

Figure 11-35 Output Power vs. Supply Voltage
PVDD=6-24V, 4ohm, PBTL，HE

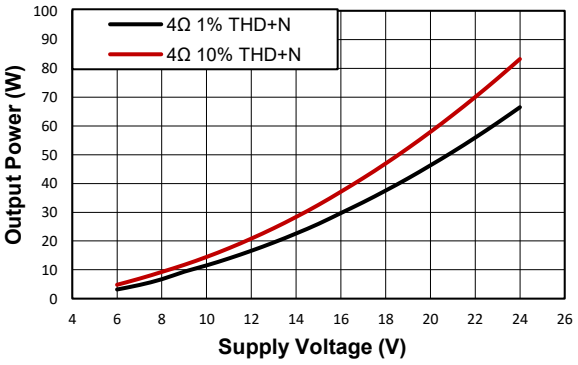

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Figure 11-36 THD+N vs. Power
PVDD=18V, 3ohm, PBTL, HE

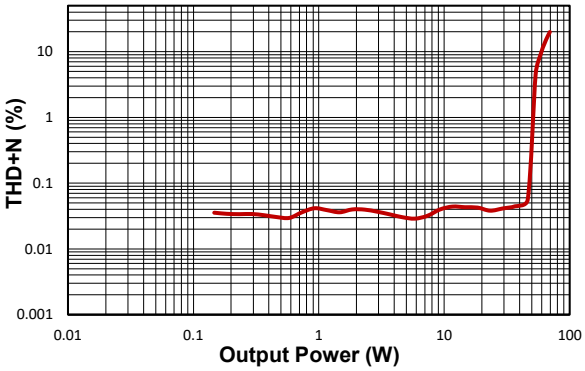

Figure 11-37 THD+N vs. Power
PVDD=24V, 3ohm, PBTL, HE

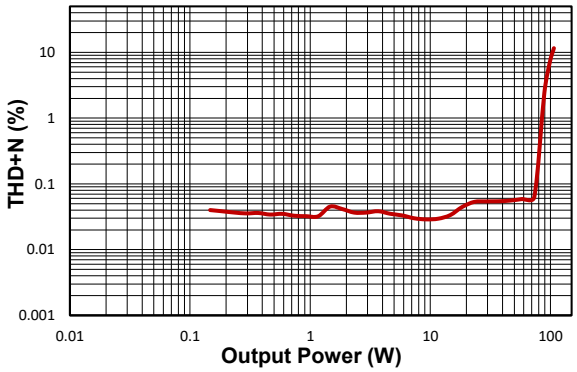

Figure 11-38 THD+N vs. Power
PVDD=24V, 4ohm, PBTL, HE

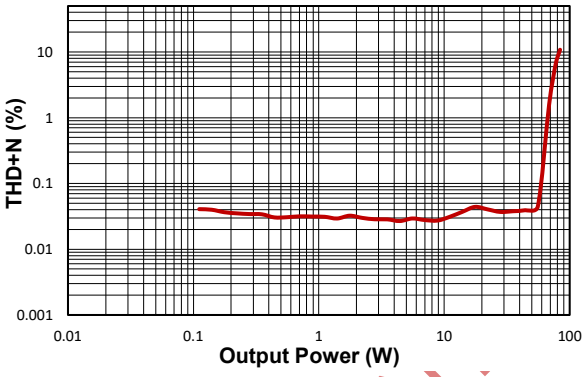

Figure 11-39 Efficiency vs. Output Power
PVDD=18V, 3ohm, PBTL, HE

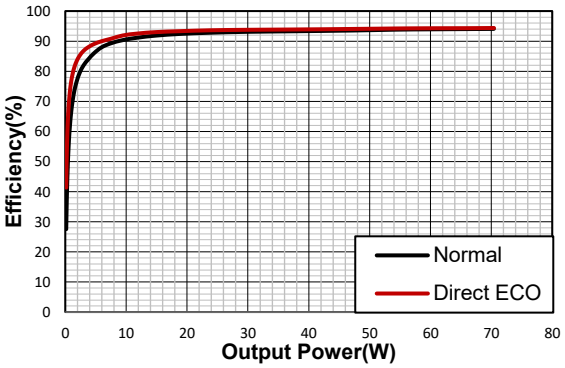

Figure 11-40 Efficiency vs. Output Power
PVDD=18V, 3ohm, PBTL, HE

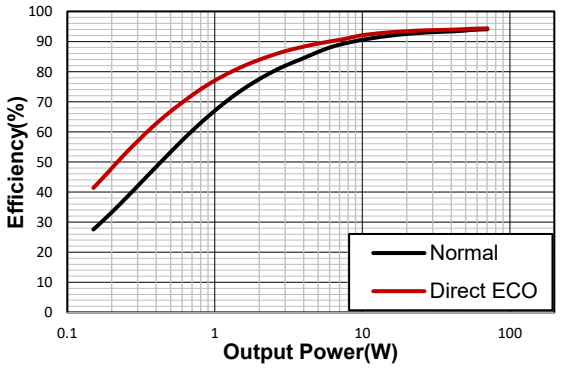

Figure 11-41 Power Loss vs. Output Power
PVDD=18V, 3ohm, PBTL, HE

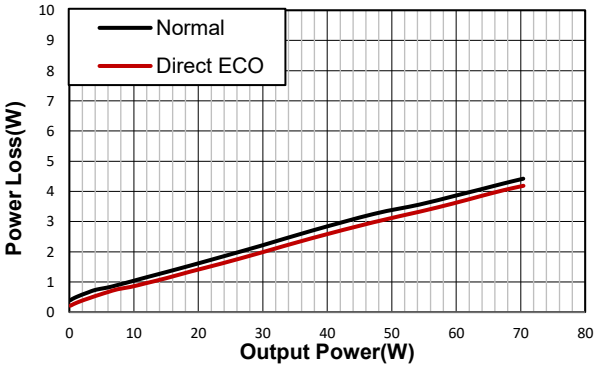

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Figure 11-42 Efficiency vs. Output Power
PVDD=24V, 3ohm, PBTL

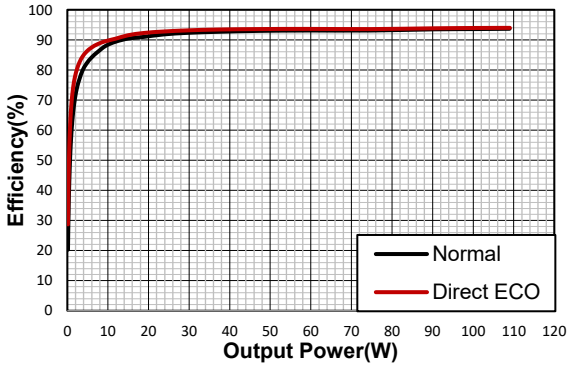


Figure 11-43 Efficiency vs. Output Power
PVDD=24V, 3ohm, PBTL

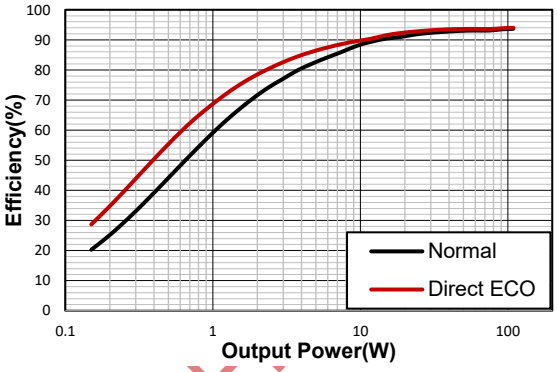


Figure 11-44 Power Loss vs. Output Power
PVDD=24V, 3ohm, PBTL

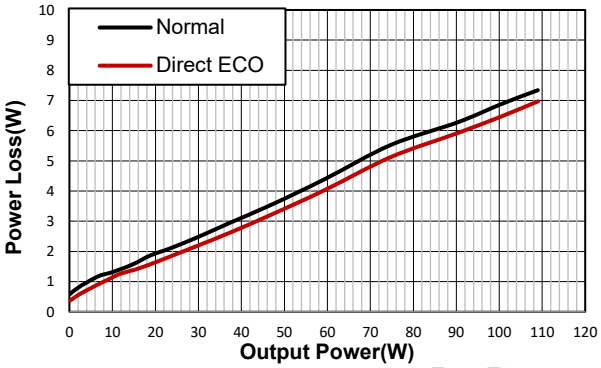


Figure 11-45 Efficiency vs. Output Power
PVDD=24V, 4ohm, PBTL, HE

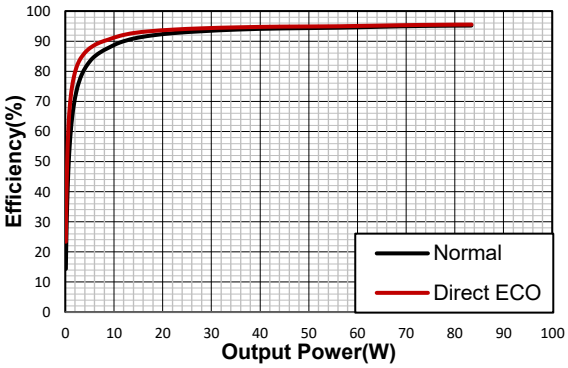


Figure 11-46 Efficiency vs. Output Power
PVDD=24V, 4ohm, PBTL, HE

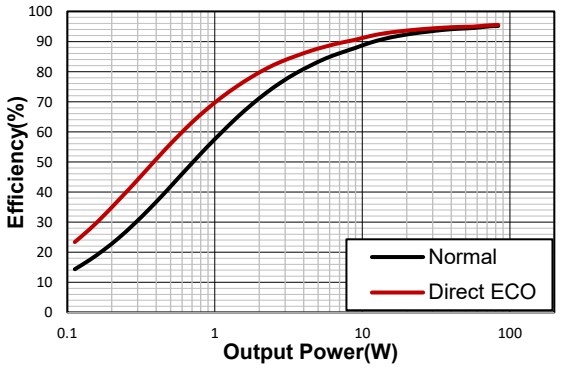
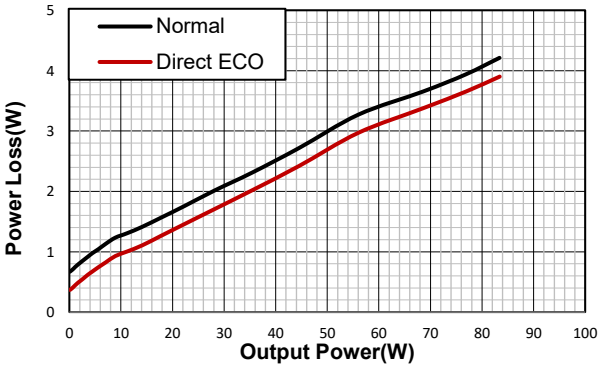


Figure 11-47 Power Loss vs. Output Power
PVDD=24V, 4ohm, PBTL, HE



12. 参数测量信息

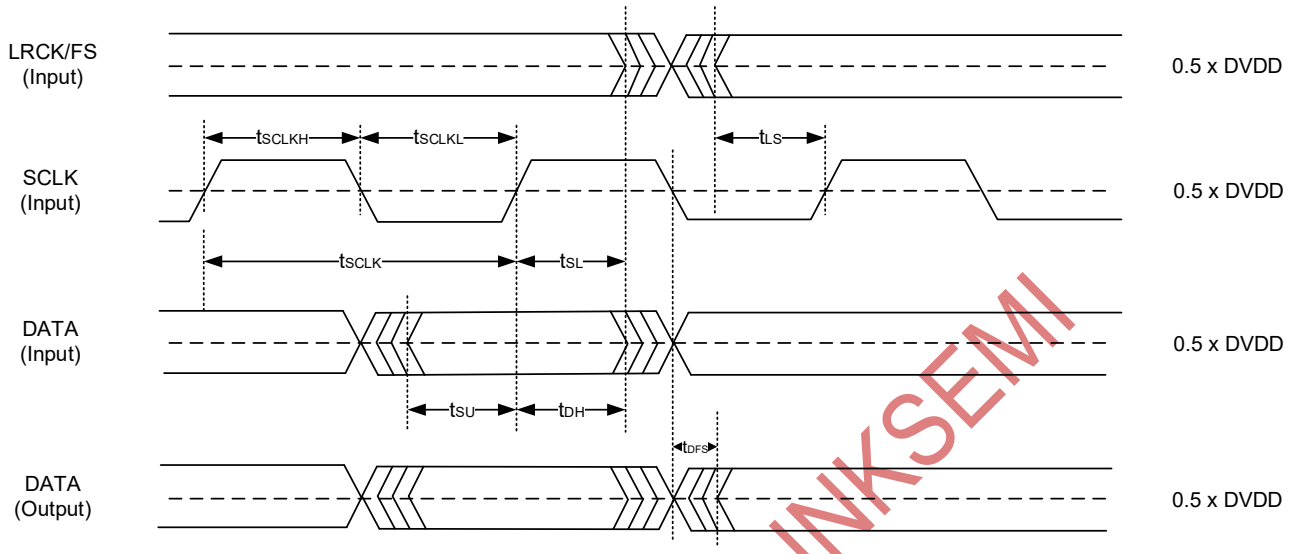


图 **12-1 Serial Audio Port Timing in Slave Mode**

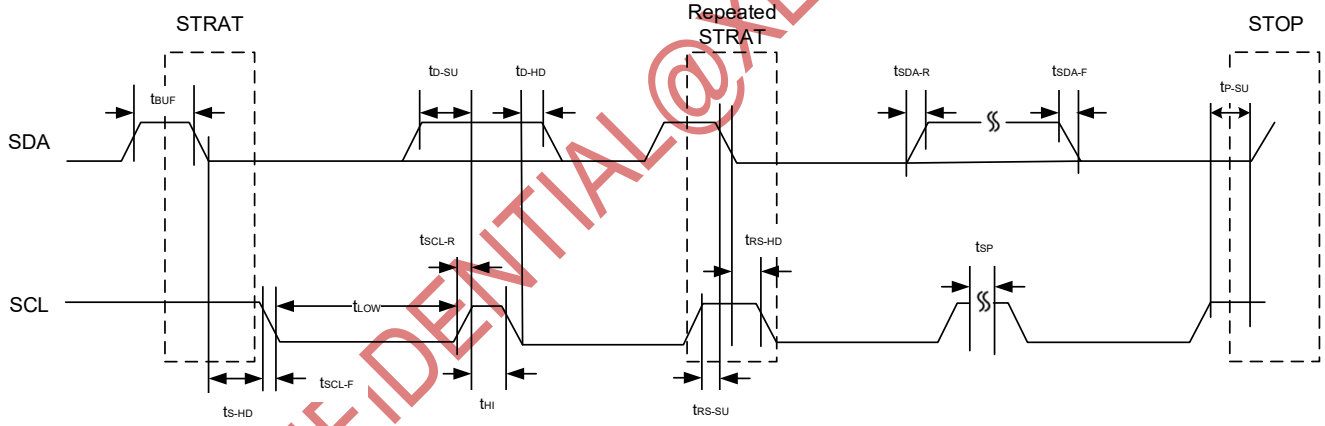


图 **12-2 I2C Communication Port Timing Diagram**

13. 详细说明

13.1. 概述

CCD6805S 主要由 5 个部分组成，包括：

1) 一个立体声 DAC
2) 32-bit 高精度音频 DSP
3) 闭环架构的 Class-D
4) I2C 控制接口
5) 保护逻辑和内部 ADC 电压温度采样模块

PVDD 供电电压范围为 4.5V 到 26.4V，DVDD 支持 3.3V 或者 1.8V 逻辑。CCD6805S 提供两个 GPIO, 可以配置成回声消除或者其他 GPIO 功能。

13.2. 功能模块框图

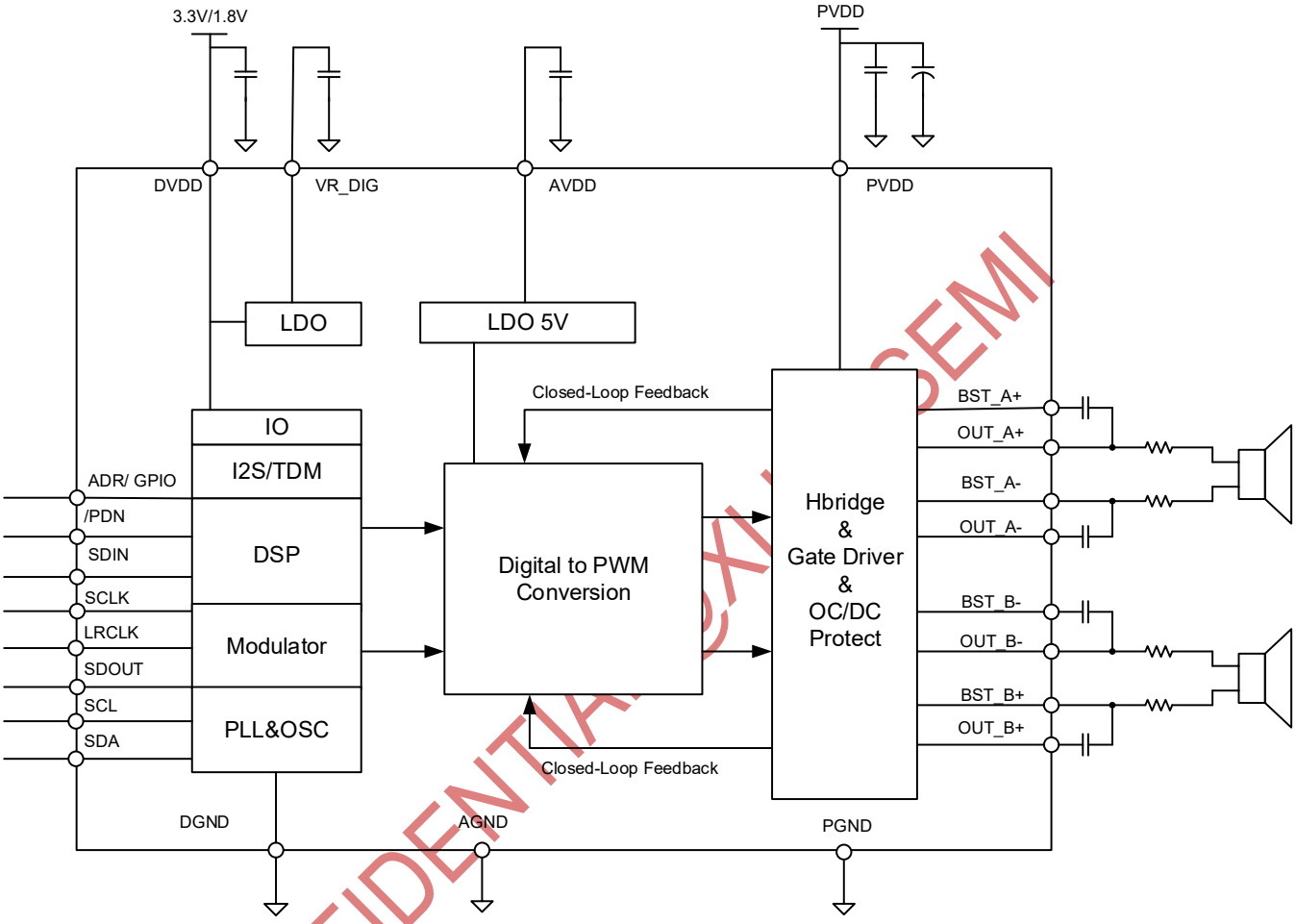


图 **13.2-1 Functional Block Diagram**

13.3. 特性描述

13.3.1. 串行音频接口几频率

CCD6805S 支持的音频输入数据格式和频率配置如下表所示：

表 **13.3.1-1 Audio Data Formats, Bit Depths, and Clock Rates**

FORMAT	DATA BITS	MAXIMUM LRCILK/FS FREQUENCY (kHz)	SCLD RATE (F_S)
I^2S/LJ/RJ	32, 24, 20,16	44.1, 48, 88.2, 96	64, 32
TDM	32, 24, 20, 16	44.1, 48	128, 256, 512
		88.2, 96	128, 256

13.3.2. 时钟停止及恢复

CCD6805S 支持时钟频率停止后自动进入 Hi-Z 或者其他低功耗模式，时钟恢复后可以自动恢复。

13.3.3. 在线改变采样率

CCD6805S 支持在线编辑 EQ 等参数，此外还支持自动切换采样率功能。通常情况为了避免 pop 音，建议进入 Hi-Z 或者 sleep 等状态后再进行采样率切换。

13.3.4. 串行音频接口-数据格式和有效位

CCD6805S 支持如下 I²S 格式：

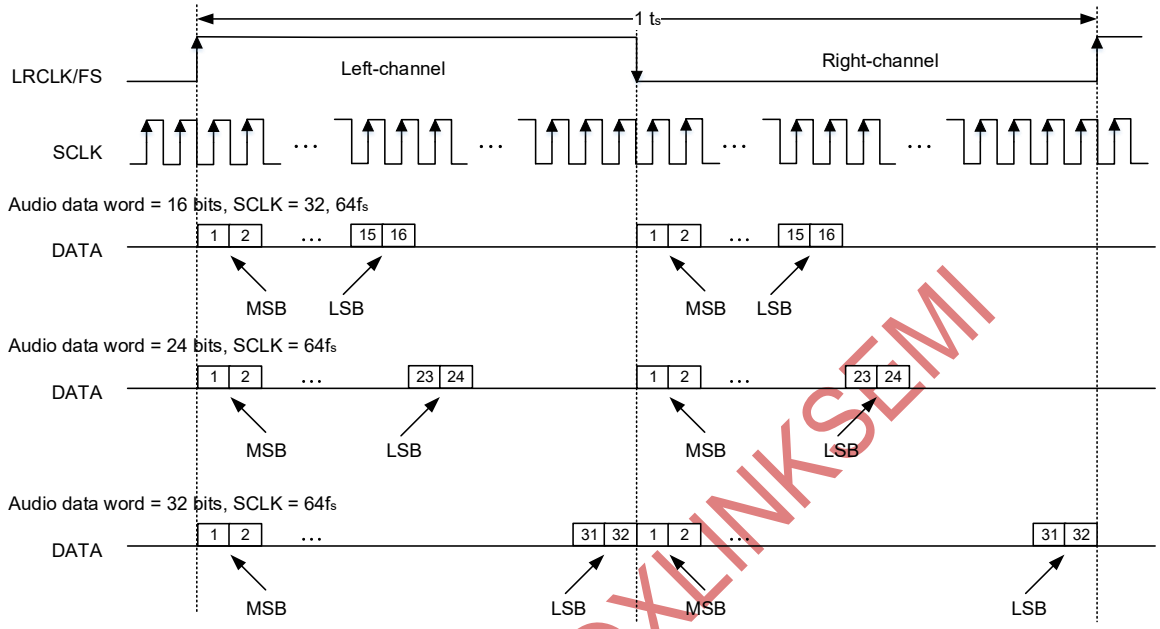


图 **13.3.4-1 Left-Justified Audio Data Format**

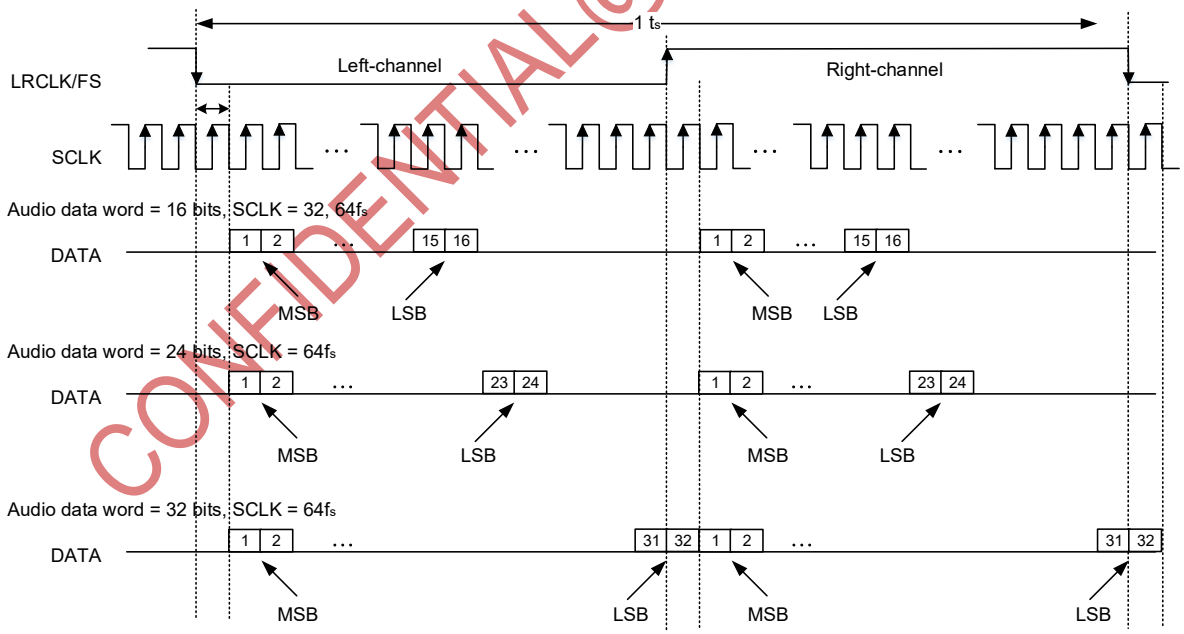


图 **13.3.4-2 I2S Audio Data Format**

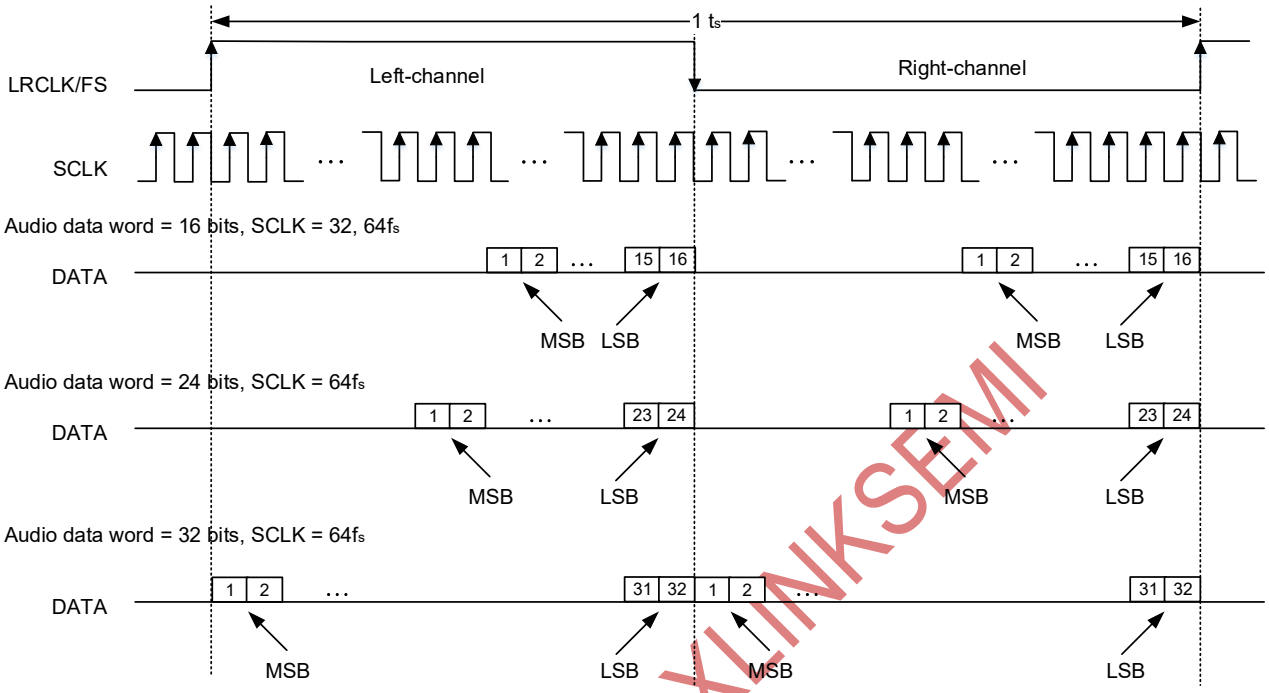
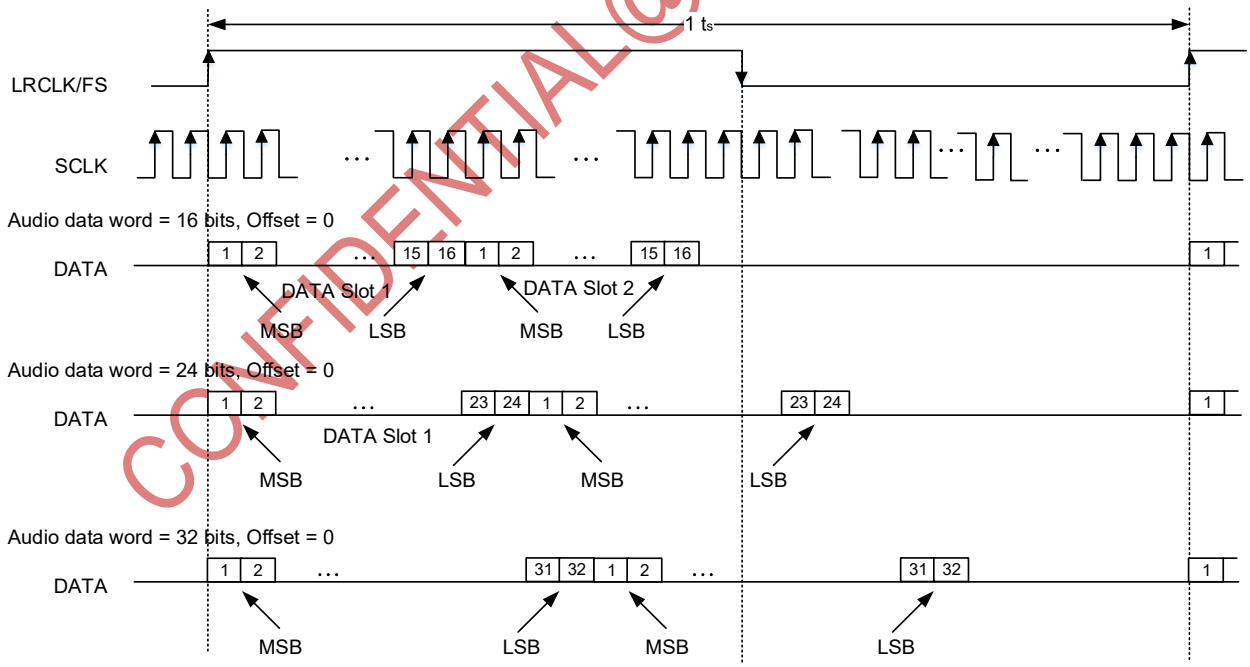
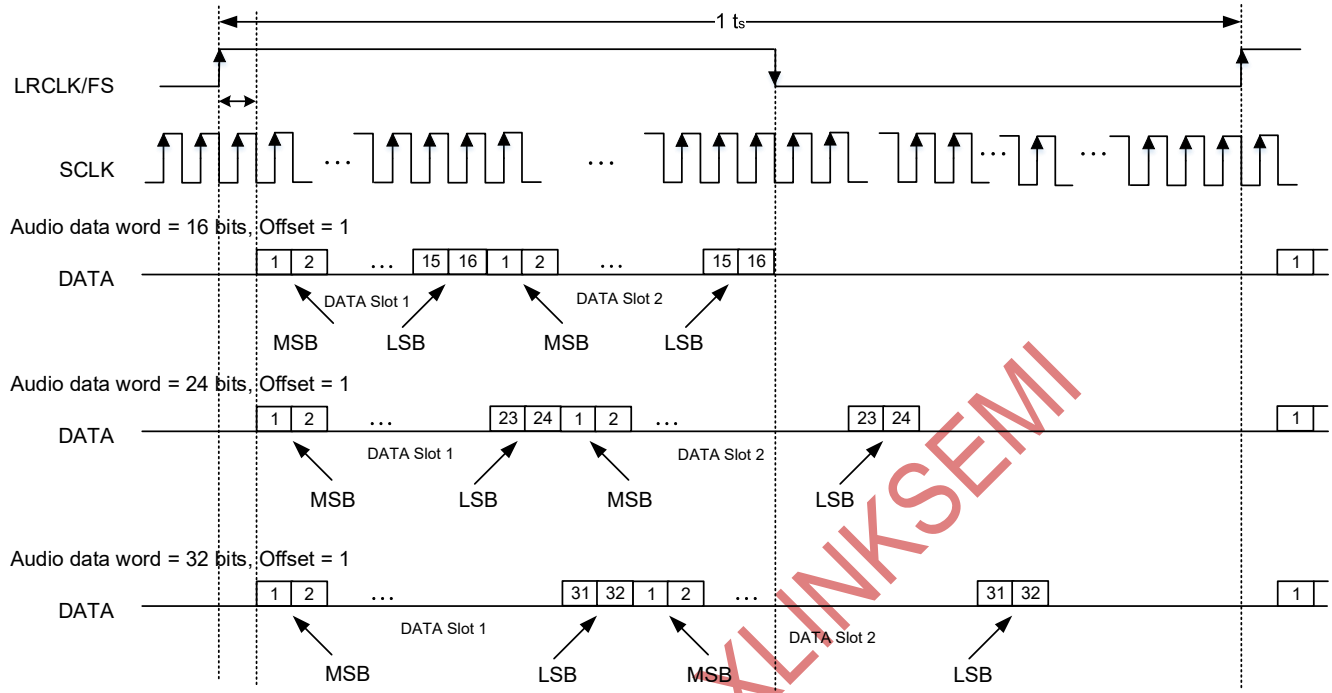


图 **13.3.4-3 Right-Justified Audio Data Format**



TDM data format with OFFSET = 0
In TDM modes, duty cycle of LRCLK/FS should be 1xSCLK at minimum. Rising edge is considered frame start.

图 **13.3.4-4 TDM 1 Audio Data Format**



TDM data format with OFFSET = 1
In TDM modes, duty cycle of LRCLK/FS should be 1xSCLK at minimum. Rising edge is considered frame start.

图 **13.3.4-5 TDM 2 Audio Data Format**

13.3.5. 数字音频处理

CCD6805S DSP 支持多种音频处理的算法结构，配置上包括立体声 2.0、高低音 1.1。 CCD6805S 提供 GUI 来方便调音过程，以下为调音算法的简要介绍

1) 2.0 模式 基础： 2 × 15 EQs +3-band DRC + AGL + 3 × post-EQ
2) 2.0 模式 高级： 2 × 15 EQs + SFS + DPEQ + 3-band DRC + AGL/ 1-band lookahead DRC + 3 × post-EQ
3) 1.1 模式： 2 × 15 EQs + SFS + DPEQ + 3-band DRC + AGL/ 1-band lookahead DRC + 3 × post-EQ + 5 × sub-EQ + sub-1band-DRC + 2 × sub-post EQ

13.3.6. 功放增益选择

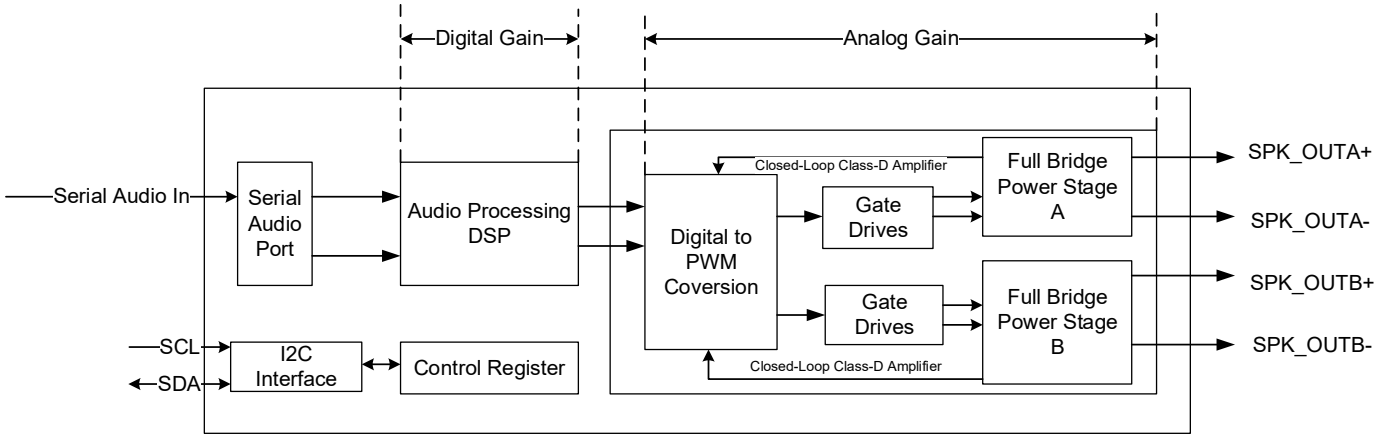


图 **13.3.6-1 Speaker Amplifier Gain**

配置增益主要通过模拟的增益，即寄存器 0x54, Book 0, Page 0。其对应的输出 peak 值如下表所示。此外，DSP 部分也可以配置增益，但是该增益受到 AGL DRC 的门限限制。

AGAIN (4:0)	GAIN (dBFS)	AMPLIFIER PEAK OUTPUT VOLTAGE (V)
00000	0	29.5
00001	-0.5	27.85
…	…	…
11111	-15.5	4.95

13.4. 器件功能模式

13.4.1. 软件控制

CCD6805S 通过 I2C 通信接口进行配置，最高支持 400kHz I2C。

13.4.1.1. BTL 模式

在 BTL 模式下，输出两路独立，分别为左声道输出和右声道输出。在信号链上看，这两路从输入、DSP 算法处理和输出都支持独立配置。CCD6805S 支持单独关闭一个通道，让另外一个通道正常工作。

13.4.1.2. PBTL 模式

CCD6805S 还可以支持 PBTL 模式（两个 BTL 模式进行并联）。在 PBTL 模式下，输出功率和输出最大电流都可以翻倍。此外，电路图上支持电感前并联或者电感后的并联，这个取决于设计峰值电流和电感饱和电流及成本之间的平衡。在驱动大功率低音炮时，通常会选择 PBTL 模式。在该模式下，信号链上一般默认选择左声道为 PBTL 输出。

13.4.2. 芯片状态控制

CCD6805S 主要有 5 种模式：

1) Shutdown: 在/PDN 拉低后，内部 LDO 都会关闭，此时功耗最低
2) Deep Sleep: I2C 正常通讯、数字核的供电正常、模拟部分 LDO 关闭、DSP 处于活动状态
3) Sleep: I2C 模块、数字核、DSP 均正常工作。此外，模拟部分 5V Analog LDO 正常工作
4) Output Hi-Z: 除了输出 power stage 外，都处于 active 状态
5) Play: 当 register 0x03h-D[1:0] = 11, 器件工作在 Play 模式

13.4.3. 芯片调制模式

13.4.3.1. BD 调制模式

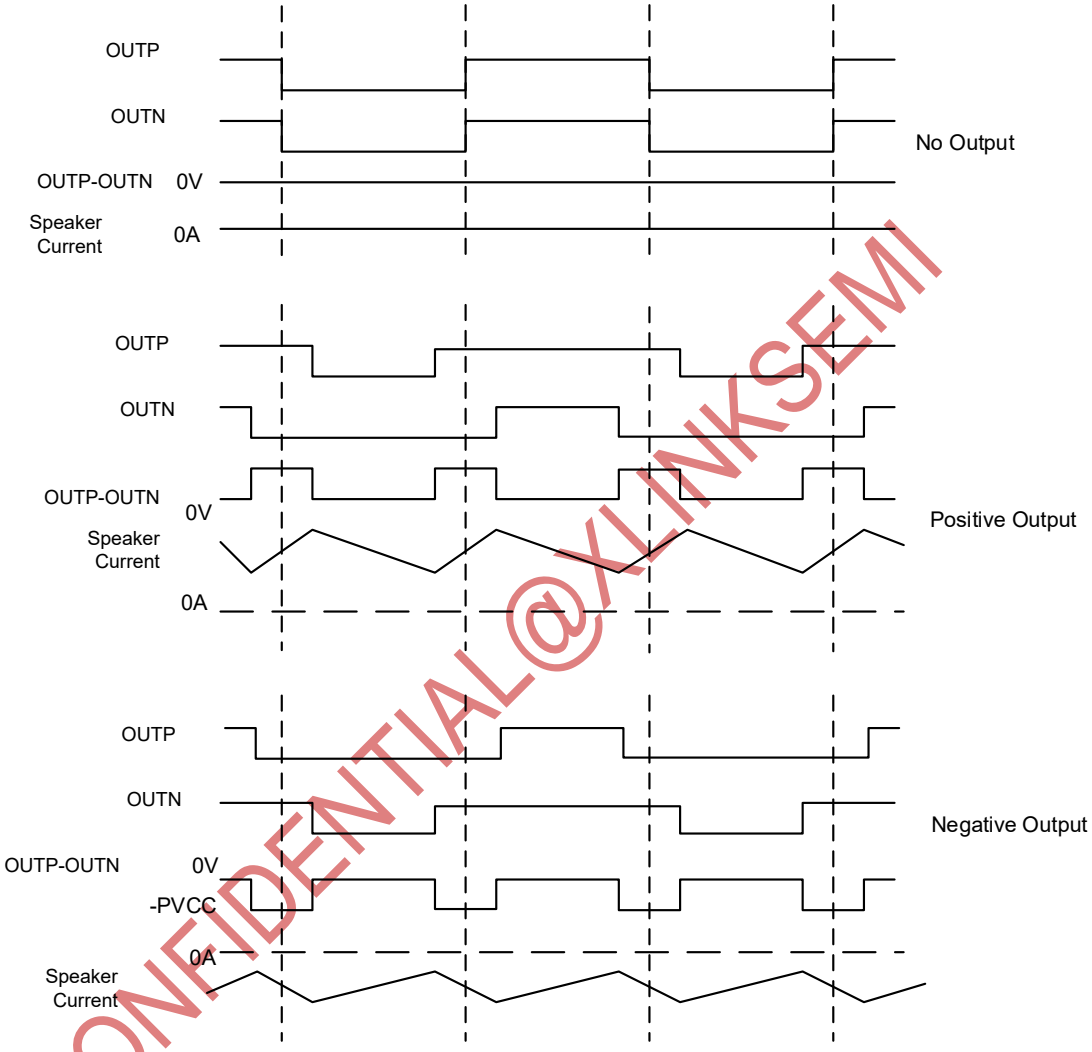


图 **13.4.3.1-1 BD Mode Modulation**

13.4.3.2. HE 调制模式

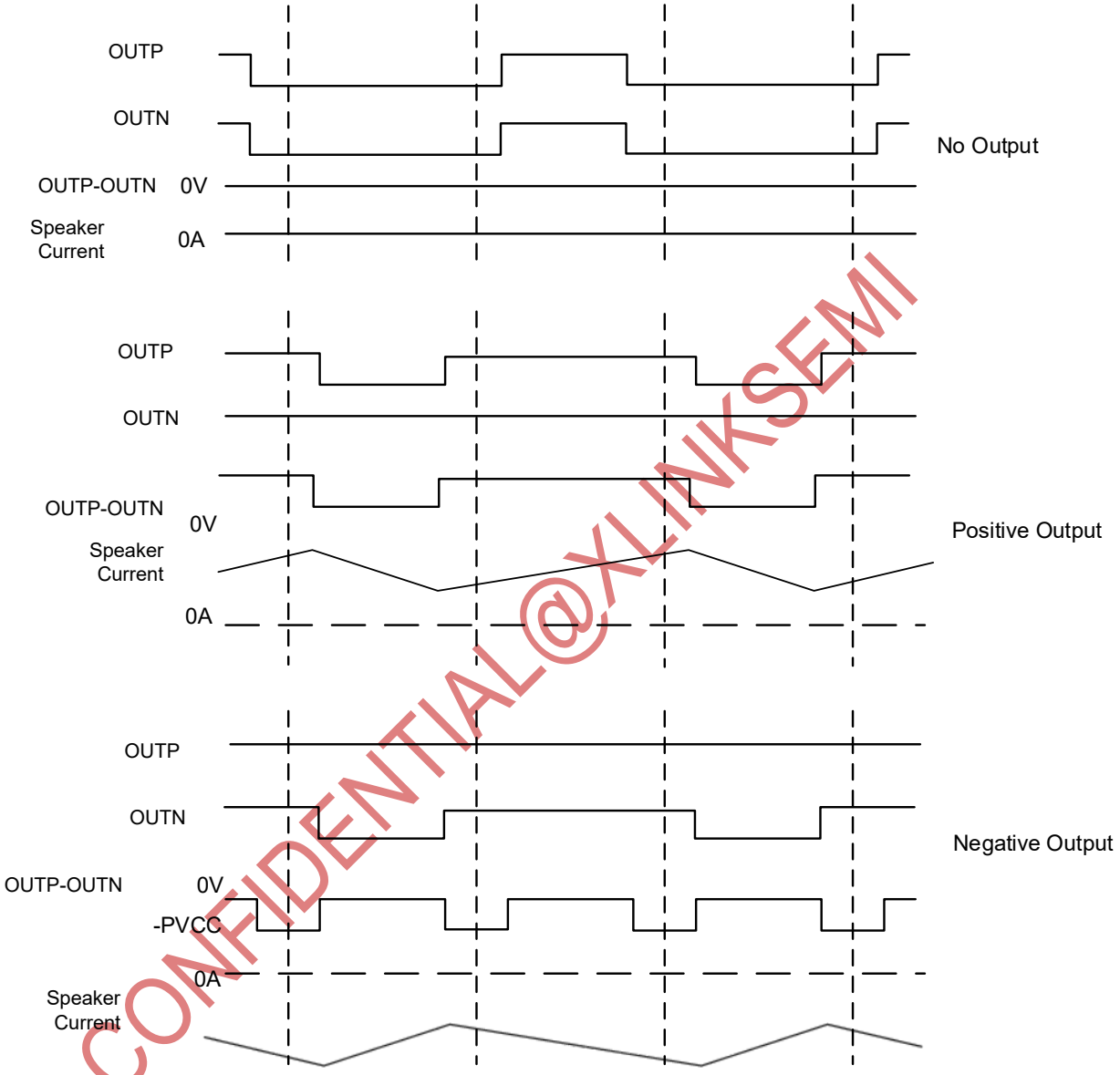


图 **13.4.3.2-1 HE Mode Modulation**

13.4.3.3. 混合调制模式（Dynamic modulation）

CCD6805S 支持混合调制模式，减小静态电流，提高效率，该模式下自动平衡 HE 模式和 BD 模式

13.5. 低功耗技术

CCD6805S 创新使用多种省电模式，这些省电模式可以叠加使用，在工作状态下，PVDD 电流低至 1mA(毫安)，相比传统模式降低一个数量级，可以极大程度延长电池使用时间和降低芯片以及 PCB 待机状态发热。

13.5.1. AVDD 直供节能模式

该模式下，AVDD 电源由外部提供，供电要求 4.85V-5.3V，芯片自动旁路内部 LDO 模块，降低发热和功耗。

13.5.2. 智感静默模式

该模式下，在芯片 PLAY 状态时，当 SDIN 线上无输入信号持续 2s 以上，芯片自动进入休眠模式，输出 PWM 关闭，此时芯片状态机仍为 PLAY 状态；当 SDIN 线上有输入信号时，无延时自动进入音乐播放；智感静默模式音乐启停过程无 pop，并且在静默过程由于功放输出级为关态，无输出噪声，无惧异常短路。

13.6. 扩频技术

CCD6805S 支持扩频技术，扩频技术能有效降低 EMI 噪音辐射。CCD6805S 支持多种不同的扩频配置，以满足不同场景的需求，相关配置请参考寄存器。

13.7. 编程和控制

13.7.1. I2C 通讯总线

CCD6805S 支持标准或者 fast I²C，标称寻址方式分为 book、page 和 register 的架构。

13.7.2. 从机地址

从机地址通过 ADR 管脚进行配置，具体如 下表所示。

ADR PIN CONFIGTATION	MSB					USER-DEFINED		LSB
4.7kΩ to DVDD (0x58)	0	1	0	1	1	0	0	R/$\overline{W}$
15kΩ to DVDD (0x5A)	0	1	0	1	1	0	1	R/$\overline{W}$
47kΩ to DVDD (0x5C)	0	1	0	1	1	1	0	R/$\overline{W}$
150kΩ to DVDD (0x5E)	0	1	0	1	1	1	1	R/$\overline{W}$

13.7.2.1. 随机写入

随机写入格式如下：

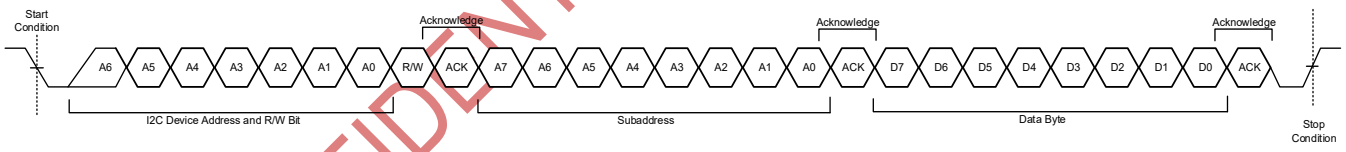


图 **13.7.2.1-1 Random Write Transfer**

13.7.2.2. 顺序写入

顺序写入格式如下：

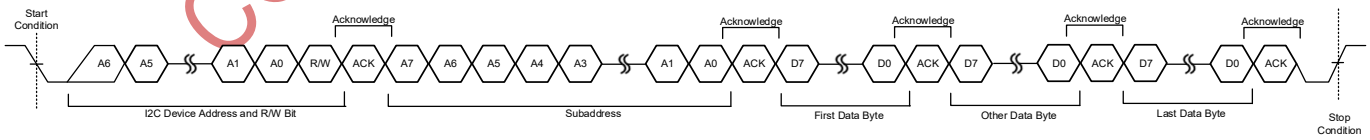


图 **13.7.2.2-1 Sequential Write Transfer**

13.7.2.3. 随机读取

随机读取格式如下：

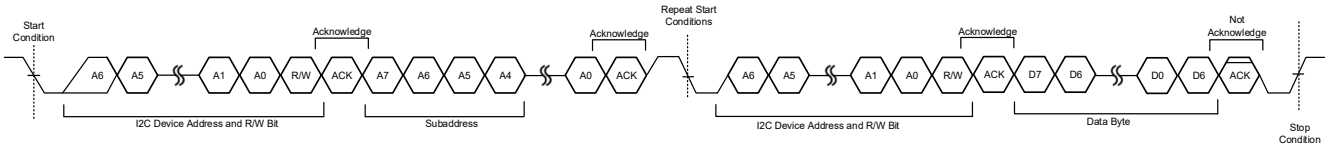


图 **13.7.2.3-1 Random Read Transfer**

13.7.2.4. 顺序读取

顺序读取格式如下：

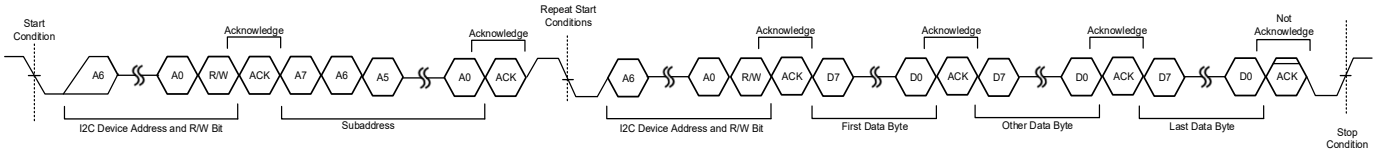


图 **13.7.2.4-1 Sequential Read Transfer**

13.7.2.5. *内存空间结构及参数更新*

CCD6805S book 操作通过 0xFE 进入相应的 book, 通过 0x00 进入相应的 page。每次切换 book，需要先进入 Page 0。 每次新进入一个 book，默认进入 Page 0。

13.7.3. 软件控制

13.7.3.1. *上电时序*

1) 配置 ADR/GPIO2 设置 I2C 地址。
2) PVDD 和 DVDD 上电。PVDD 和 DVDD 无上电时序先后要求。
3) PVDD 和 DVDD 上电完成 1ms 后，拉/PDN。
4) /PDN 拉高后等待 1ms，然后配置 I2C 进入 play。I2C 配置过程中间无需插入延迟时间，且不需要 I2S 时钟存在。

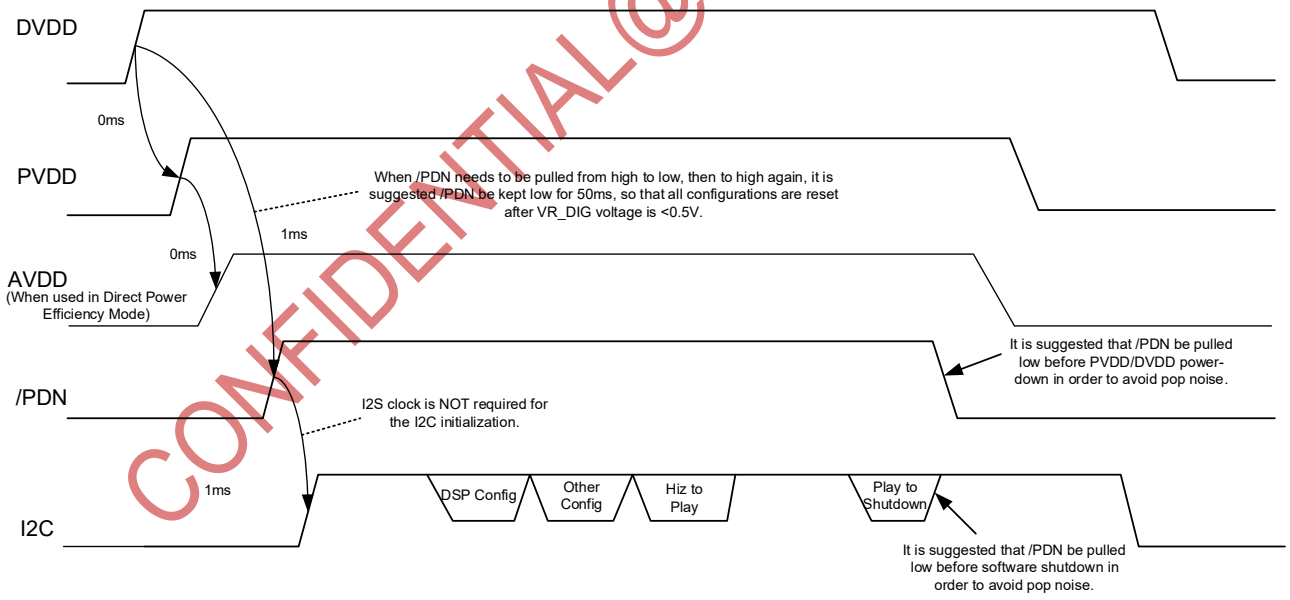


图 **13.7.3.1-1 Start-up and Power-Down Sequence**

13.7.3.2. *下电时序*

1) 芯片正常工作
2) 配置寄存器让芯片进入 Hi-Z 或以下的状态，然后拉低 PDN
3) 等待 10ms
4) 拉低 PVDD，再拉低 DVDD
5) 芯片处于下电状态

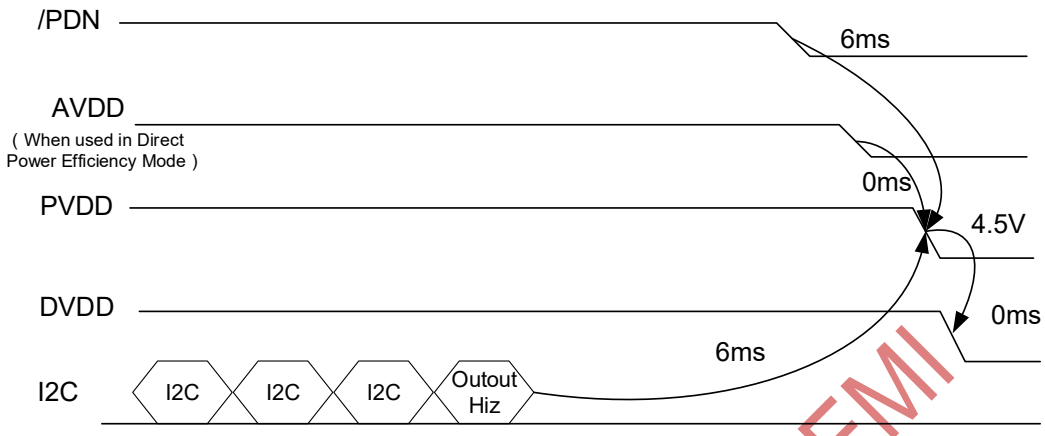


图 **13.7.3.2-1 Power-Down Sequence**

在 PVDD 和 DVDD 掉电之前，建议提前至少 6ms 软件关闭输出，比如在进入 Hi-Z 模式之后拉低 PDN，这样可以有效的 避免掉电 pop 音。

13.7.3.3. 保护和监测

13.7.3.3.1. 过流关断保护（**OCSD**）

在严重短路事件（例如输出短路到 PVDD 或 GND，或者喇叭短路）下，可能会导致输出两个通道任一通道存在瞬时大电流，如果该瞬时大电流超过芯片过流保护门限，则芯片将会在 100ns 内关闭芯片两个通道。过流关断速度取决于多种因素，例如短路阻抗、电源电压和开关频率，触发过流保护后，芯片不会自动重启，用户可以通过 I2C 重新启动芯片进入工作状态。OCSD 事件发生后，ADR/GPIO2 拉低，并且 I2C 相应寄存器可以读到相应错误。

13.7.3.3.2. 扬声器直流保护（**DC**）

如果芯片输出级直流偏移电压超过扬声器直流保护门限 （典型值 1.9V），并且持续超过 600ms，ADR/GPIO2 引脚会被触发拉低并且芯片两路输出关闭进入 Hi-Z 状态，该错误状态也会记录在 Book0/Page0 中的寄存器 0x70 中，且该错误状态不会自动恢复，需要软件手动配置 0x78 寄存器清除 fault 后，才可以重新进入播放状态。

13.7.3.3.3. 器件过热保护（**OTSD**）

一旦芯片温度超过器件过热保护门限（典型值 160℃），器件会将输出驱动器从播放模式设置为高阻抗模式。 Book0/Page0 中的寄存器 0x72 报告过温关机故障。此故障的行为设置为自动恢复模式，一旦芯片温度降至 150°C，器件将自动返回播放模式，用户也 可以通过清除 Book0/Page0 中的寄存器 0x78 的故障记录来重新进入播放模式。

13.7.3.3.4. 过压和欠压保护 （**OV/UV**）

13.7.3.3.4.1. 过压保护 （OV）

一旦 PVDD 电压超过过压保护门限 （典型值 28V），芯片将从播放模式进入 Hi-Z 模式，并且 Book0/Page0 中的寄存器 0x71 报告过压故障。一旦过压保护事件消失，芯片将自动返回播放模式。但是寄存报错记录需要通过 Book0/Page0 中的寄存器 0x78 清除，否则该错误标志位仍保持为 1。

13.7.3.3.4.2. 欠压保护 （UV）

一旦 PVDD 电压降至欠压保护门限 （典型值 4V）以下，芯片将从播放模式进入 Hi-Z 模式，并且 Book0/Page0 中的 寄存器 0x71 报告过压故障。一旦欠压保护事件消失，芯片将自动返回播放模式。但是寄存报错记录需要通过 Book0/Page0 中的寄存器 0x78 清除，否则该错误标志位仍保持为 1。

13.7.3.3.5. **I2S** 时钟错误 （**Clock Fault**）

时钟一般是由于外部输入的 I2S 时钟发生 Clock 信号停止、SCLK/LRCLK 比例错误、LRCLK 时钟频率不符合标准等情况导致。芯片的 Book0/Page0 寄存器 0x37 和寄存器 0x39 会实时监测时钟状态，如果有错，会通过寄存器 0x71 报出。 Clock fault 可以在寄存器 0x71 中读取。

14. 寄存器列表

Table of regmap

RESET CTRL Register (8'h1) [Reset = 0x00]

RESET CTRL Register (8'h1) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[4]	RST DIG CORE	W	0x0	WRITE CLEAR BIT Reset DIG_CORE WRITE CLEAR BIT Reset Full Digital Core. This bit resets the Full Digital Signal Path (Include DSP coefficient RAM and I2C Control Port Registers), Since the DSP is also reset, the coefficient RAM content is also cleared by the DSP. 0: Normal 1: Reset Full Digital Signal Path
[0]	RST REG	W	0x0	WRITE CLEAR BIT Reset Registers This bit resets the mode registers back to their initial values. Only reset Control Port Registers, The RAM content is not cleared. 0: Normal 1: Reset I2C Control Port Registers

DEVICE CTRL1 Register (8'h2) [Reset = 0x10]

DEVICE CTRL1 Register (8'h2) [Reset = 0x10]				
Bit	Field	Type	Reset	Description
[7]	DAMP PBTL	RW	0x0	0: set damp to btl mode 1: set damp to pbtl mode updated when not in play state
[6:4]	FSW SEL	RW	0x1	select fsw 000:384k 001:260k 010:480k 011:576k 100:310k 101:768k 110:310k 111:768k
[1:0]	DAMP MOD	RW	0x0	00:BD mode 01:HE mode 10: Hybrid mode updated when not in play state

DEVICE CTRL2 Register (8'h3) [Reset = 0x10]

DEVICE CTRL2 Register (8'h3) [Reset = 0x10]				
Bit	Field	Type	Reset	Description
[4]	DSP RST	RW	0x1	DSP reset When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation 1: Reset the DSP
[3]	CH1 MUTE	RW	0x0	Mute Left Channel This bit issues soft mute request for the left channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
[2]	CH2 MUTE	RW	0x0	Mute Right Channel This bit issues soft mute request for the right channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
[1:0]	STATE CTL	RW	0x0	device state control register 00: Deep Sleep, 01: Sleep, 10: Hiz, 11: PLAY

I2C PAGE AUTO INC Register (8'hf) [Reset = 0x00]

I2C PAGE AUTO INC Register (8'hf) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[3]	PAGE AUTOINC REG	RW	0x0	Page auto increment disable Disable page auto increment mode. for non -zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0 the location of current page itself like in older part. 0: Enable Page auto increment 1: Disable Page auto increment

SDOUT SEL Register (8'h30) [Reset = 0x00]

SDOUT SEL Register (8'h30) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[1:0]	SDOUT SEL	RW	0x0	Open-drain selection [1] This bit selects Open-drain mode for sdout pin 0: Push pull 1: Open drain SDOUT Select [0] This bit selects what is being output as SDOUT via GPIO pins. 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

I2S CTRL Register (8'h31) [Reset = 0x00]

I2S CTRL Register (8'h31) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[5]	SCLK INV	RW	0x0	BCK Polarity This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally they are assumed to be aligned to the falling edge of the BCK. 0: Normal BCK mode 1: Inverted BCK mode

SAP CTRL1 Register (8'h33) [Reset = 0x02]

SAP CTRL1 Register (8'h33) [Reset = 0x02]				
Bit	Field	Type	Reset	Description
[7]	I2S SHIFT MSB	RW	0x0	Audio Shift MSB
[5:4]	DATA FORMAT	RW	0x0	I2S Data Format These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: DSP 10: RTJ 11: LTJ
[3:2]	I2S LRCLK PULSE	RW	0x0	01: lrclk pulse<8 SCLK
[1:0]	WORD LENGTH	RW	0x2	Audio Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

SAP CTRL2 Register (8'h34) [Reset = 0x00]

SAP CTRL2 Register (8'h34) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[7:0]	I2S SHIFT	RW	0x0	Audio Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio sample. 000000000: offset = 0 BCK (no offset) 000000001: offset = 1 BCK 000000010: offset = 2 BCKs … 111111111: offset = 512 BCKs eg: H34 = H01, H33 = H13 (TDM8 SLOT0 32BIT)

SAP CTRL3 Register (8'h35) [Reset = 0x11]

SAP CTRL3 Register (8'h35) [Reset = 0x11]				
Bit	Field	Type	Reset	Description
[5:4]	LEFT DAC DPATH	RW	0x1	Left DAC Data Path These bits control the left channel audio data path connection. 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
[1:0]	RIGHT DAC DPATH	RW	0x1	Right DAC Data Path These bits control the right channel audio data path connection. 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)

DSP PGM MODE Register (8'h40) [Reset = 0x01]

DSP PGM MODE Register (8'h40) [Reset = 0x01]				
Bit	Field	Type	Reset	Description
[4:0]	HIZ SEL	RW	0x1	[4]: Right Channel HIZ [3]: Left Channel HIZ [2:0] reserved Note: Those bits are associated with BIT H50 for being used in ultra low idle current applications

DSP CTRL Register (8'h46) [Reset = 0x00]

DSP CTRL Register (8'h46) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[7]	RESERVED	RW	0x0	RESERVED
[4:3]	USER DEFINE PROCESSING RATE	RW	0x0	00: flow follow input FS 01: 96K input FS, using 48K dsp process flow
[1:0]	RESERVED	RW	0x0	RESERVED

DIG VOL RIGHT Register (8'h4C) [Reset = 0x30]

DIG VOL RIGHT Register (8'h4C) [Reset = 0x30]				
Bit	Field	Type	Reset	Description
[7:0]	POST GAIN LEFT	RW	0x30	Right Digital Volume These bits control the right channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB … 00101111: +0.5 dB 00110000: 0.0 dB 00110001: -0.5 dB ... 11111110: -103 dB 11111111: Mute

DIG VOL LEFT Register (8'h4D) [Reset = 0x30]

DIG VOL LEFT Register (8'h4D) [Reset = 0x30]				
Bit	Field	Type	Reset	Description
[7:0]	POST GAIN RIGHT	RW	0x30	Left Digital Volume These bits control the left channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB … 00101111: +0.5 dB 00110000: 0.0 dB 00110001: -0.5 dB ... 11111110: -103 dB 11111111: Mute

DIG VOL CTRL2 Register (8'h4E) [Reset = 0x33]

DIG VOL CTRL2 Register (8'h4E) [Reset = 0x33]				
Bit	Field	Type	Reset	Description

[7:6]	POST GAIN RAMP DOWN SPEED	RW	0x0	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
[5:4]	POST GAIN RAMP DOWN STEP	RW	0x3	Digital Volume Normal Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
[3:2]	POST GAIN RAMP UP SPEED	RW	0x0	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
[1:0]	POST GAIN RAMP UP STEP	RW	0x3	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up. 00: Increment by 4 dB for each update 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update 11: Increment by 0.5 dB for each update

AUTO MUTE CTRL Register (8'h50) [Reset = 0x07]

AUTO MUTE CTRL Register (8'h50) [Reset = 0x07]				
Bit	Field	Type	Reset	Description
[3]	POWERSAVE MODE	RW	0x0	0: Disable auto power save mode 1: Enable auto power save mode
[2:0]	AUTO MUTE CTRL	RW	0x7	bit0: 0: Disable left channel auto mute 1: Enable left channel auto mute bit1: 0: Disable right channel auto mute 1: Enable right channel auto mute bit2: 0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted. Note: Those bits are associated with BIT H40 for being used in ultra low idle current applications

AUTO MUTE TIME Register (8'h51) [Reset = 0x00]

AUTO MUTE TIME Register (8'h51) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[6:4]	AUTOMUTE TIME LEFT	RW	0x0	Auto Mute Time for Left Channel These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
[2:0]	AUTOMUTE TIME RIGHT	RW	0x0	Auto Mute Time for Right Channel These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms

				100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

AGAIN Register (8'h54) [Reset = 0x00]

AGAIN Register (8'h54) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[4:0]	ANA GAIN	RW	0x0	Analog Gain Control This bit controls the right channel analog gain. 00000: 0 dB 00001: -0.5db …... 11111: -15.5 dB

GPIO CTRL Register (8'h60) [Reset = 0x00]

GPIO CTRL Register (8'h60) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[2]	GPIO2 OE	RW	0x0	GPIO2 Output Enable. This bit sets the direction of the GPIO2 pin 0: GPIO2 is input 1: GPIO2 is output
[1]	RESERVED	RW	0x0	RESERVED
[0]	GPIO1 OE	RW	0x0	GPIO0 Output Enable This bit sets the direction of the GPIO0 pin 0: GPIO1 is input 1: GPIO1 is output

GPIO0 SEL Register (8'h61) [Reset = 0x00]

GPIO0 SEL Register (8'h61) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[4:0]	GPIO1 SEL(PIN9)	RW	0x0	0000: off (low) 0001: Reserved 0010: Reserved 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock missing) 0111: Reserved 1000: GPIO1 as WARNZ output 1001: Serial audio interface data output (SDOUT) 1010: classh_sdout 1011: GPIO1 as FAULTZ output 1100: pvdd_uv_det 1101: Reserved 1110: Reserved 1111: Reserved

GPIO2 SEL Register (8'h63) [Reset = 0x00]

GPIO2 SEL Register (8'h63) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[4:0]	GPIO2 SEL(PIN3)	RW	0x0	0000: off (low) 0001: Reserved 0010: Reserved 0011: Auto mute flag (asserted when both L and R channels are auto muted) 0100: Auto mute flag for left channel 0101: Auto mute flag for right channel 0110: Clock invalid flag (clock error or clock missing) 0111: Reserved 1000: GPIO2 as WARNZ output 1001: Serial audio interface data output (SDOUT) 1010: classh_sdout 1011: GPIO2 as FAULTZ output 1100: pvdd_uv_det 1101: Reserved 1110: Reserved 1111: Reserved

GPIO INPUT SEL Register (8'h64) [Reset = 0x00]

GPIO INPUT SEL Register (8'h64) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[3:2]	GPIO RESETZ SEL	RW	0x0	00/10: N/A 01: GPIO1 11: GPIO2 cannot be reset by GPIO reset
[1:0]	GPIO MUTEZ SEL	RW	0x0	00/10: N/A 01: GPIO1 11: GPIO2 MUTEZ pin active-low, output driver sets to HiZ state, the output stop switching of the Class D amplifier.

GPIO OUT Register (8'h65) [Reset = 0x00]

GPIO OUT Register (8'h65) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[2:0]	GPIO OUT	RW	0x0	bit0: GPIO1 output bit1: RESERVED bit2: GPIO2 output

GPIO OUT INV Register (8'h79) [Reset = 0x00]

GPIO OUT INV Register (8'h79) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[6:4]	GPIO OUT OD EN	RW	0x0	GPIO opendrain enable
[2:0]	GPIO OUT INV	RW	0x0	bit0: GPIO1 output invert bit1: RESERVED bit2: GPIO2 output invert

POWER STATE Register (8'h68) [Reset = 0x00]

POWER STATE Register (8'h68) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[1:0]	STATE RPT	RO	0x0	0: Deep sleep, 1: Seep 2: HIZ 3: Play others: reserved

AUTOMUTE STATE Register (8'h69) [Reset = 0x00]

AUTOMUTE STATE Register (8'h69) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[1]	ZERO RIGHT MON	RO	0x0	This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted
[0]	ZERO LEFT MON	RO	0x0	This bit indicates the auto mute status for left channel. 0: Not auto muted 1: Auto muted

RAMP SS CTRL0 Register (8'h6B) [Reset = 0x00]

RAMP SS CTRL0 Register (8'h6B) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[2]	SS HIGH LEVEL SEL	RW	0x0	0: triangle freq 1/16 fsw 1: random (1/16: 16/16) *(1/16) fsw
[1]	SS RDM EN	RW	0x0	random SS enable
[0]	SS TRI EN	RW	0x0	triangle SS enable

RAMP SS CTRL1 Register (8'h6C) [Reset = 0x03]

RAMP SS CTRL1 Register (8'h6C) [Reset = 0x03]				
Bit	Field	Type	Reset	Description
[5:4]	SS RDM CTRL	RW	0x0	random SS range control 00: range 0 01: range 1 10: range 2 11: range 3 Note: range3 > range2 > range1 > range0
[1:0]	SS TRI CTRL	RW	0x3	triangle SS frequency and range control 00:2.5% 01:5%

				10:7.5% 11:10%

CHAN FAULT Register (8'h70) [Reset = 0x00]

CHAN FAULT Register (8'h70) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[3]	CH1 DC	RO	0x0	CHA (CH1) DC error report
[2]	CH2 DC	RO	0x0	CHB (CH2) DC error report
[1]	CH1 OC	RO	0x0	CHA (CH1) over current error report
[0]	CH2 OC	RO	0x0	CHB (CH2) over current error report

GLOBAL FAULT1 Register (8'h71) [Reset = 0x00]

GLOBAL FAULT1 Register (8'h71) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[2]	CLK FAULT	RO	0x0	
[1]	PVDD OV	RO	0x0	
[0]	PVDD UV	RO	0x0	

GLOBAL FAULT2 Register (8'h72) [Reset = 0x00]

GLOBAL FAULT2 Register (8'h72) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[0]	OTSD	RO	0x0	OT shutdown

GLOBAL FAULT3 Register (8'h73) [Reset = 0x00]

GLOBAL FAULT3 Register (8'h73) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[3]	OTW LEVEL HIGH	RO	0x0	OTW 150
[2]	OTW LEVEL LOW	RO	0x0	OTW 135

PIN CONTROL1 Register (8'h74) [Reset = 0x00]

PIN CONTROL1 Register (8'h74) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[7]	MASK OTSD	RW	0x0	Mask OTSD error report
[6]	MASK DVDD UV	RW	0x0	Mask DVDD UV error report
[5]	MASK DVDD OV	RW	0x0	Mask DVDD OV error report
[4]	MASK CLK FAULT	RW	0x0	Mask CLK FAULT error report
[3]	MASK PVDD UV	RW	0x0	Mask PVDD UV error report
[2]	MASK PVDD OV	RW	0x0	Mask PVDD OV error report
[1]	MASK DC	RW	0x0	Mask OUTPUT DC error report
[0]	MASK OC	RW	0x0	Mask OUTPUT OC error report

PIN CONTROL2 Register (8'h75) [Reset = 0x38]

PIN CONTROL2 Register (8'h75) [Reset = 0x38]				
Bit	Field	Type	Reset	Description
[5]	CLKFLT LATCH EN	RW	0x1	Enable Clock fault latch
[4]	OTSD LATCH EN	RW	0x1	Enable OTSD latch
[3]	OTW LATCH EN	RW	0x1	Enable OTW latch
[2]	MASK OTW	RW	0x0	Mask OTW report

MISC CONTROL Register (8'h76) [Reset = 0x00]

MISC CONTROL Register (8'h76) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[7]	RESERVED	RW	0x0	RESERVED
[4]	OTSD AUTO REC EN	RW	0x0	0: OTSD no auto recovery 1: OTSD auto recovery
[0]	RESERVED	RW	0x0	RESERVED

FAULT CLEAR Register (8'h78) [Reset = 0x00]

FAULT CLEAR Register (8'h78) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[7]	ANA FAULT CLEAR	W	0x0	WRITE CLEAR BIT once write this bit to 1, device clears analog fault

DSP MISC1 Register (8'h80) [Reset = 0x02]

DSP MISC1 Register (8'h80) [Reset = 0x02]

Bit	Field	Type	Reset	Description
[7:0]	DSP FLOW CTRL	RW	0x02	[7]: reserved [6]: reserved [5]: reserved [4]: reserved [3]: reserved [2]: reserved [1]: bypass subchannel [0]: reserved

DSP MISC Register (8'h66) [Reset = 0xCF]

DSP MISC Register (8'h66) [Reset = 0xCF]				
Bit	Field	Type	Reset	Description
[7]	DSP DIS CLASSH	RW	0x1	[7]: Class H_disable
[6]	DSP DIS DPEQ	RW	0x1	[6]: Bypass DPEQ
[5]	DSP DIS AGL	RW	0x0	[5]: Replace AGL by lookahead DRC
[4]	RESERVED	RW	0x0	RESERVED
[3]	DSP GANG EQ	RW	0x1	[3]: Gang EQ
[2]	DSP DIS SPATIALIZER	RW	0x1	[2]: Bypass SPATIALIZER
[1]	DSP DIS DRC	RW	0x1	[1] Bypass DRC
[0]	DSP DIS EQ	RW	0x1	[0]: Bypass EQ

DIG VOL CTRL1 Register (8'h90) [Reset = 0x00]

DIG VOL CTRL1 Register (8'h90) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[1:0]	POST GAIN CTL SEL	RW	0x0	Digital Volume Control These bits control the behavior of the digital volume. 00: The volume for Left and right channels are independent 01: Right channel volume follows left channel setting 10: Left channel volume follows right channel setting 11: Reserved (The volume for Left and right channels are independent)

DRBOOST CTRL1 Register (8'h92) [Reset = 0xF9]

DRBOOST CTRL1 Register (8'h92) [Reset = 0xF9]				
Bit	Field	Type	Reset	Description
[0]	HDR ON	RW	0x1	1: DR BOOST enable

DRBOOST CTRL6 Register (8'h97) [Reset = 0x00]

DRBOOST CTRL6 Register (8'h97) [Reset = 0x00]				
Bit	Field	Type	Reset	Description
[7:4]	RESERVED	RW	0x0	RESERVED
[3:2]	RESERVED	RW	0x0	RESERVED
[1:0]	HDR THRESHOLD	RW	0x0	threshold 00: -54db 01: -36db 10: -72db 11: -102db

15. 应用

15.1. 自举电容

建议使用 0.22μF-0.47μF 的电容用于自举电容，通常建议使用 0.47μF。

15.1.1. 电感选型

一般情况建议选择电感组合 10μH + 0.68μF 的组合，如果对静态电流有进一步要求，请参考如下建议。通常电感选型有四个关键参数：分别为电感感值、电感饱和电流、电感直流阻抗以及电感的线性度。首先电感值和饱和电流主要考虑如下几个公式：

1) 在输出启动瞬间，占空比会根据不同模式从 0 增加到 θ。

$$I_{peak\_power\_up} \approx PVDD \times \sqrt{C/L} \times \sin\left(1//\sqrt{L \times C} \times \theta/F_{SW}\right) \quad (1)$$

其中：

- θ = 0.5 （BD 模式），或 0.14 （HE 模式）。

公式（1）可以作为上电启动瞬间触发过流保护的选型参考，需要保证 $I_{peak\_power\_up}$ 低于过流保护门限。

PVDD	L(μH)	C(μF)	F_{SW} (kHz)	$I_{peak\_power\_up}$
24	4.7	0.68	384	6.07A(>5A OCP), not recommended
24	4.7	0.68	768	3.25A
24	10	0.68	384	3A
24	10	0.68	768	1.55A
12	4.7	0.68	384	3.32A
12	10	0.68	384	1.55A

2) 在播放模式下，音乐信号可能会导致输出削波，此时最坏情况引起最大电流为：

$$I_{peak\_power\_up} \approx PVDD \times (1-\theta)/(F_{SW} \times L) \quad (2)$$

3) 最大功率下流过电感电流为：

$$I_{peak\_power\_up} = \sqrt{2 \times Max\_Outout\_Power/P_{Speaker\_load}} \quad (3)$$

综合上述三个公式，建议电感饱和电流大于上述三个数值最大值，并且建议保留 30%左右的裕量。此外，最小感值建议如下表所示。

PVDD(V)	SWITCHING FREQUENCY (kHz)	MODULATION SCHEME	RECOMMENDED MINIMUM INDUCANCE(μF) FOR LC FILTER DESIGN
≤12	384	BD	4.7μH + 0.68μF
＞12			10μH + 0.68μF
≤12	384	HE	10μH + 0.68μF
＞12			15μH + 0.68μF

如果选择更高的开关频率，建议最小感值大于等于 384kHz / FSW × L。

15.1.2. 供电去耦电容设计

推荐每组 PVDD 使用 10μF 并联 0.1μF 电容用于高频滤波，且电容必须靠近左右通道各自的 PVDD，以形成电容到地的最小回路。

15.1.3. 输出 EMI 滤波设计

出于 EMI 考虑，CCD6805S 集成了高阶的展频配合硬件电路设计。详细参数设置，请联系技术支持。

15.2. 典型应用

15.2.1. BTL 模式

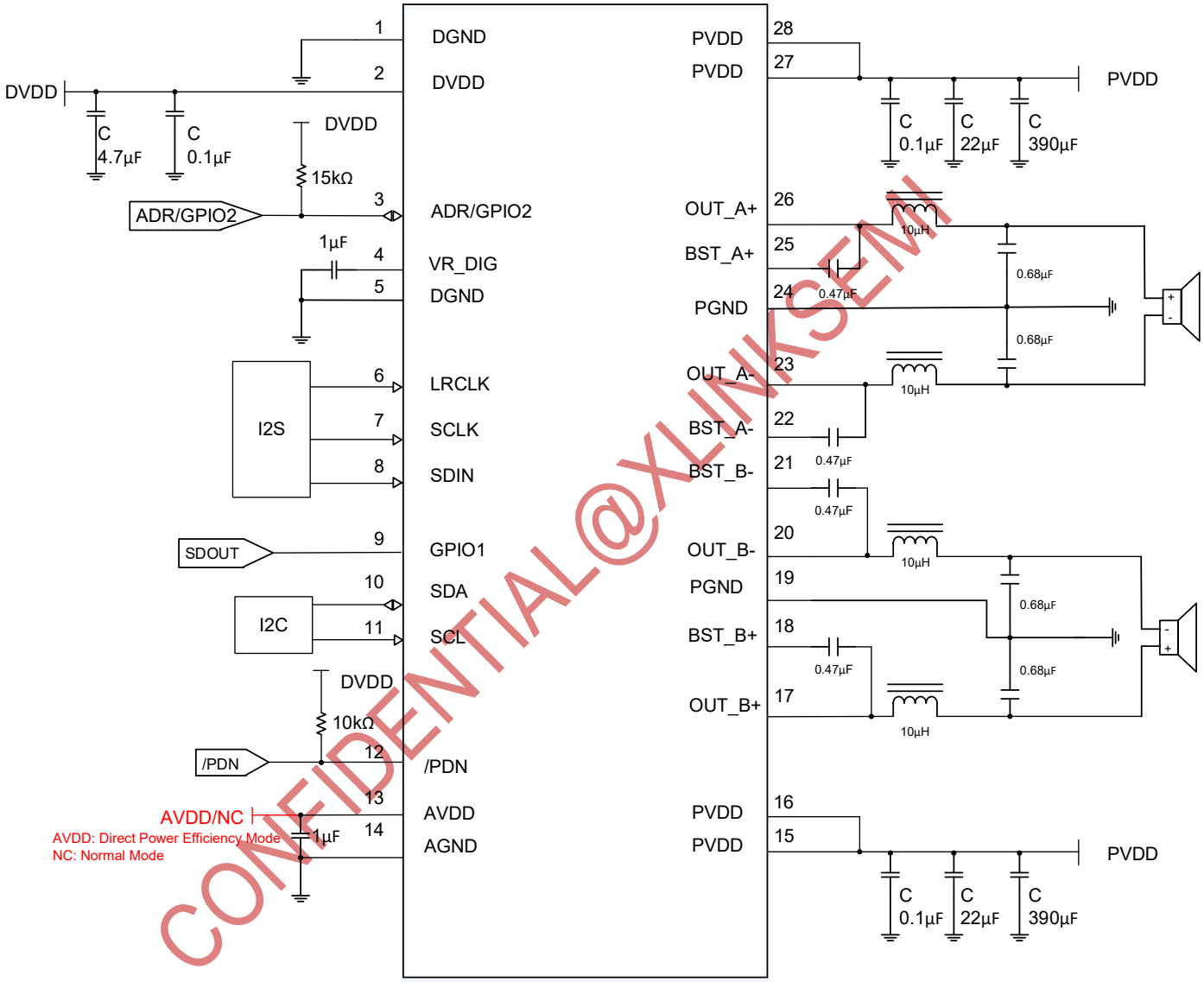


图 **15.2.1-1 BTL System Application Schematic**

15.2.2. PBTL 模式

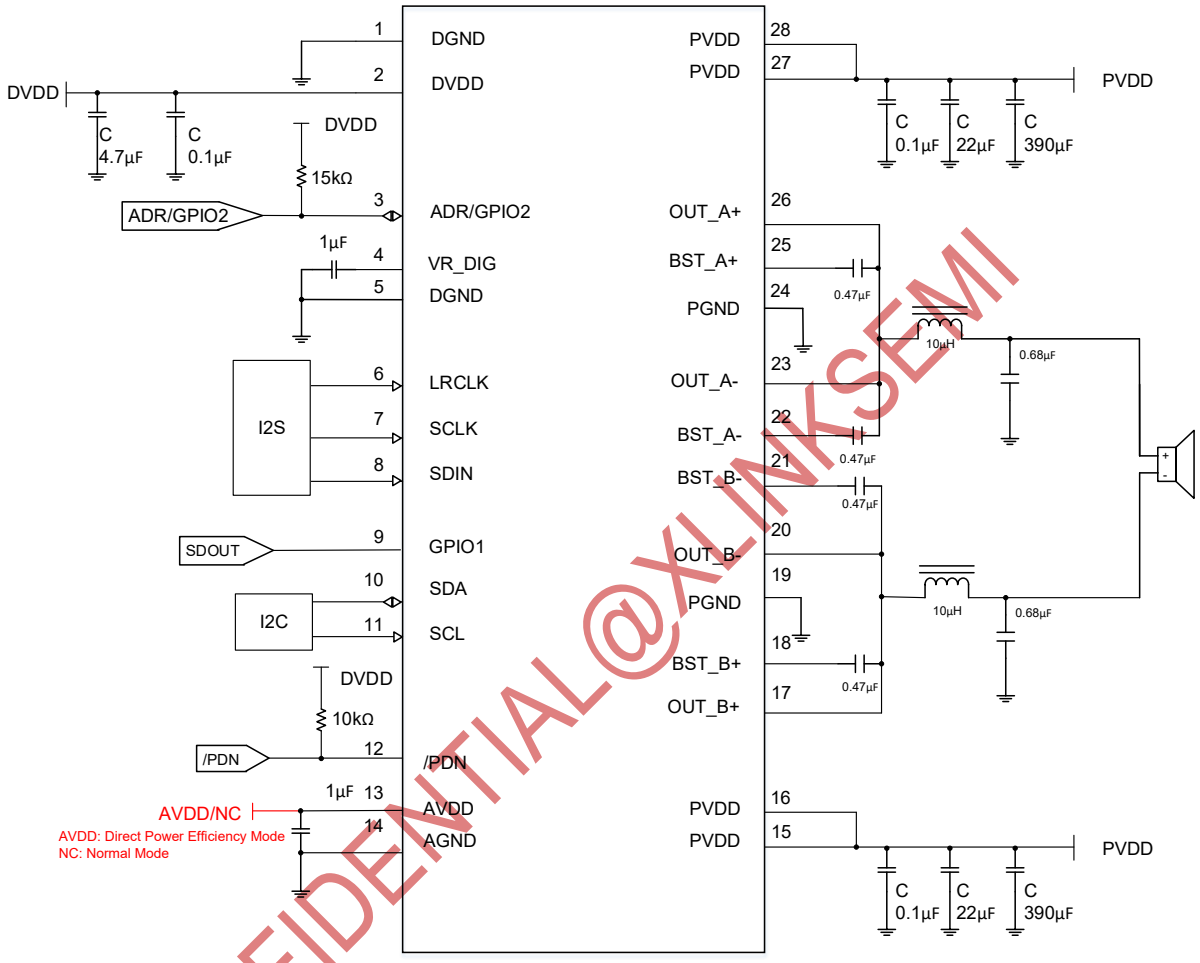


图 **15.2.1-1 PBTL System Application Schematic**

16. 供电推荐

16.1. DVDD 供电

DVDD 支持 3.3V 和 1.8V，通常建议使用 0.1μF 电容加 4.7μF 电容作为去耦。

16.2. PVDD 供电

PVDD 支持范围为 4.5V-26.4V，一般建议每组 PVDD 使用 10μF 并联 0.1μF 电容用于高频滤波，且电容必须靠近 PVDD，以形成电容到地的最小回路。

16.3. AVDD 供电

传统模式时，AVDD 由内部 LDO 产生，外接 Bypass 电容产生偏置电压， 无需外部电源。

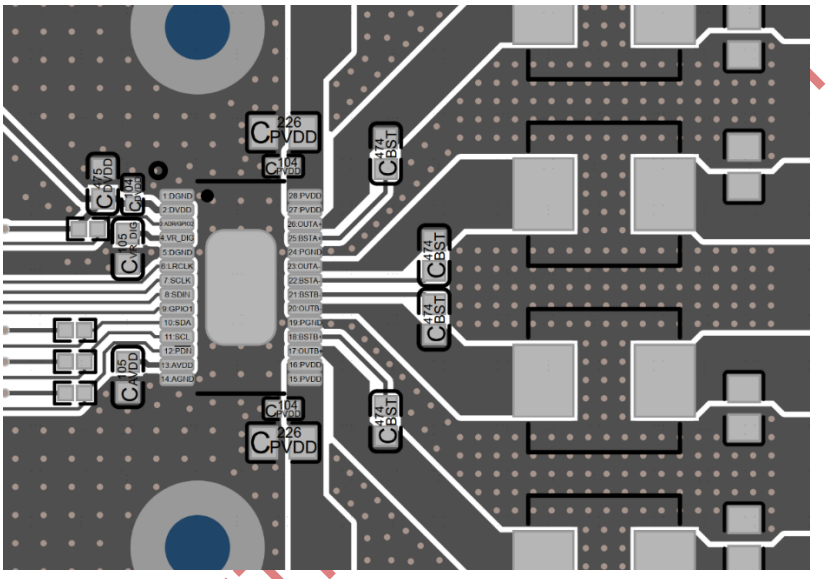
直供节能模式（Direct ECO mode)时，AVDD 外部供电 4.85v-5.3v，此模式可以降低 PVDD 上的静态功耗，显著降低芯片待机时候的功耗。

16.4. Layout

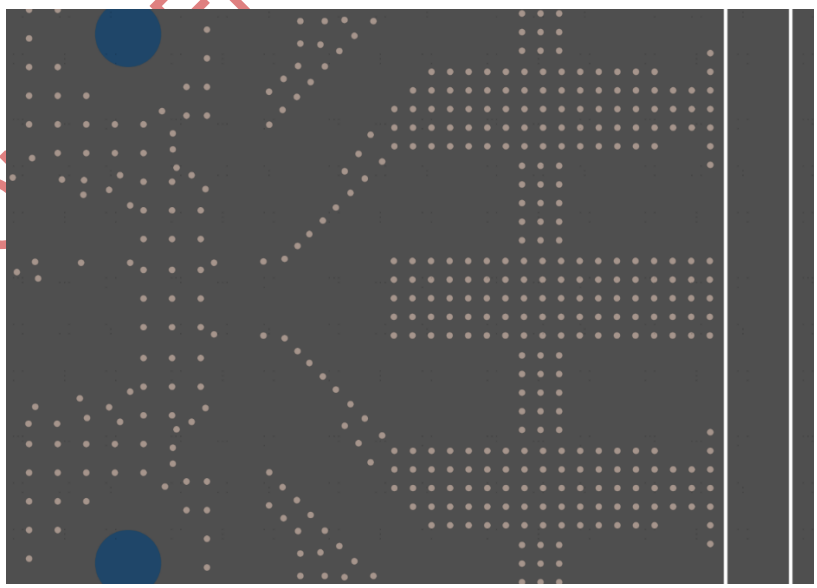
两层板布局，单侧元器件摆放布局参考如下：

1) PVDD 退耦电容靠经芯片 PVDD pin 和 GND pin 形成最短回路
2) 尽可能延展地平面，不要有断层，增加各层过孔，保证 PCB 最佳散热环境
3) 芯片 GND pin 周围必须要有足够的过孔，以及地平面，起到降低阻抗和增强散热的作用
4) DVDD, AVDD 退耦电容方式参考 PVDD 退耦电容要求
5) 对散热要求特别高的应用，可以底面开窗固定散热片散热
6) 参考设计底层全部为地平面

16.4-1 表层设计



16.4-2 底层设计



17. 封装信息

图 **17-1** 封装图

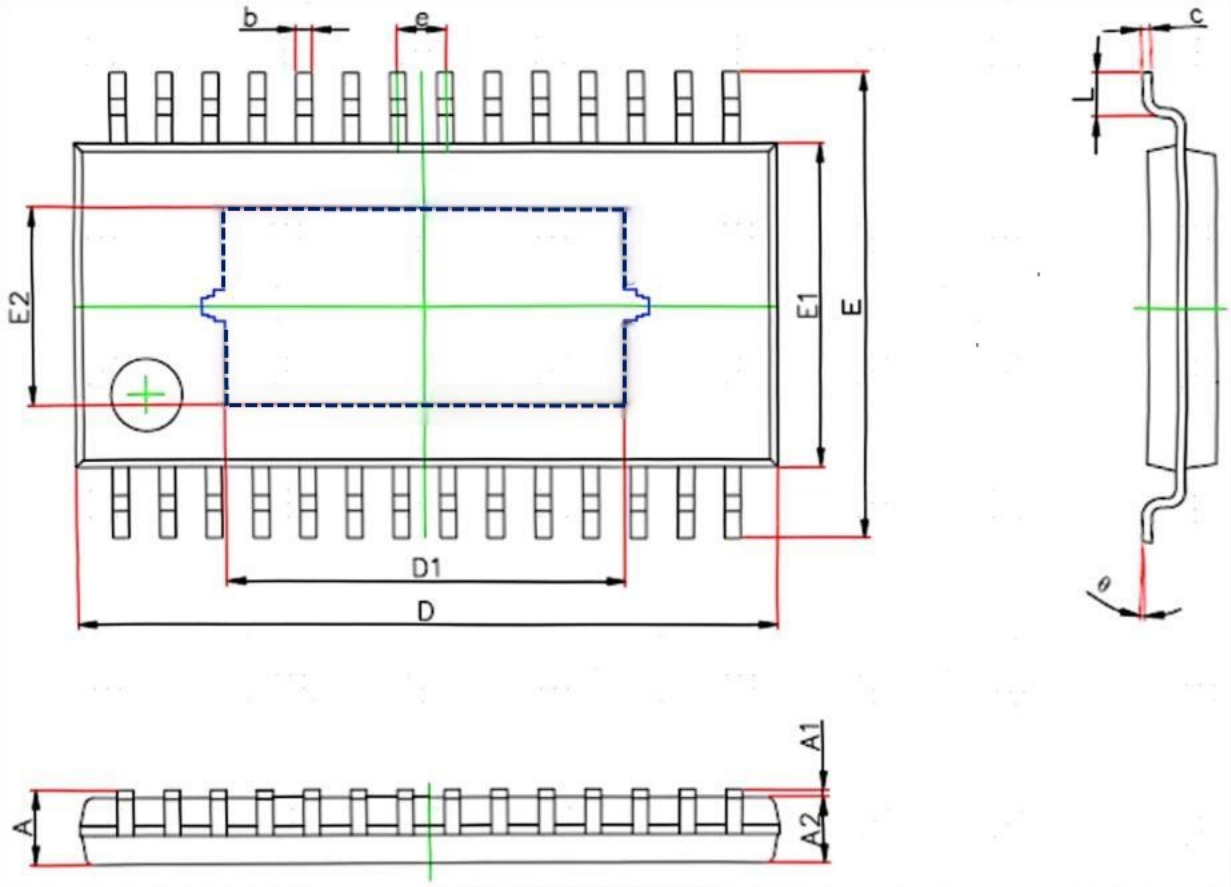
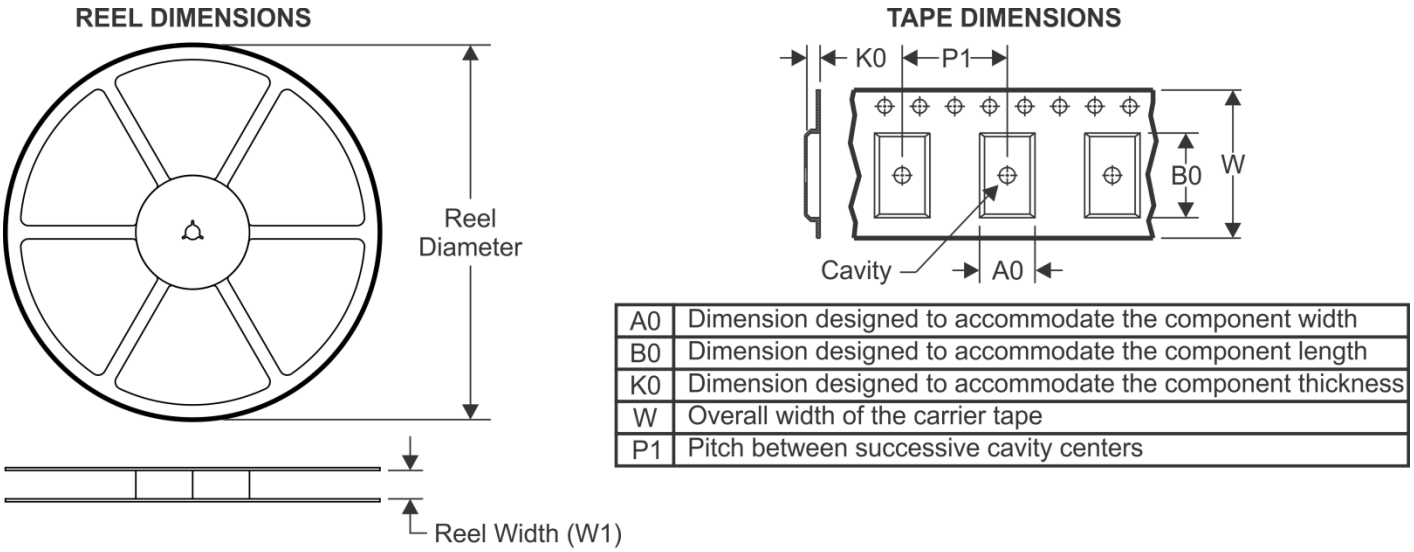


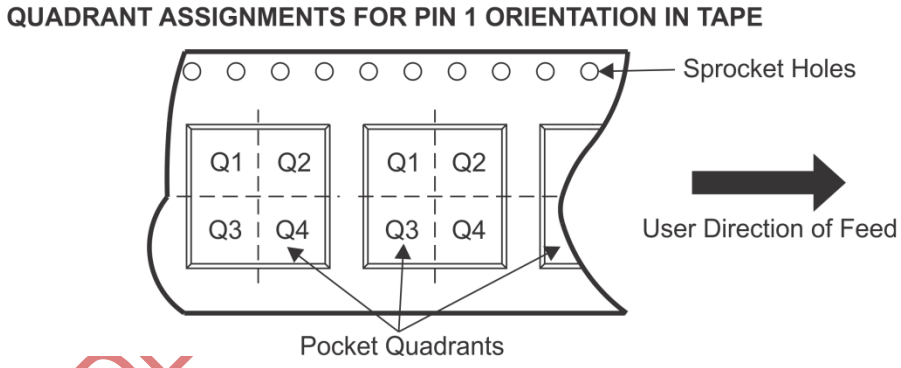
Table 17-1 封装数据

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.200			0.047
A1	0.050	-	0.150	0.002		0.006
A2	0.800		1.050	0.031		0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D	9.600		9.800	0.378		0.386
D1	5.990		6.190	0.236		0.244
E	6.250		6.550	0.246		0.258
E1	4.300		4.500	0.169		0.177
E2	2.650		2.850	0.104		0.112
e		0.650(BSC)			0.650(BSC)	
L	0.450		0.750	0.018		0.030
θ	0°		8°	0°		8°

图 **17-2** 卷盘信息

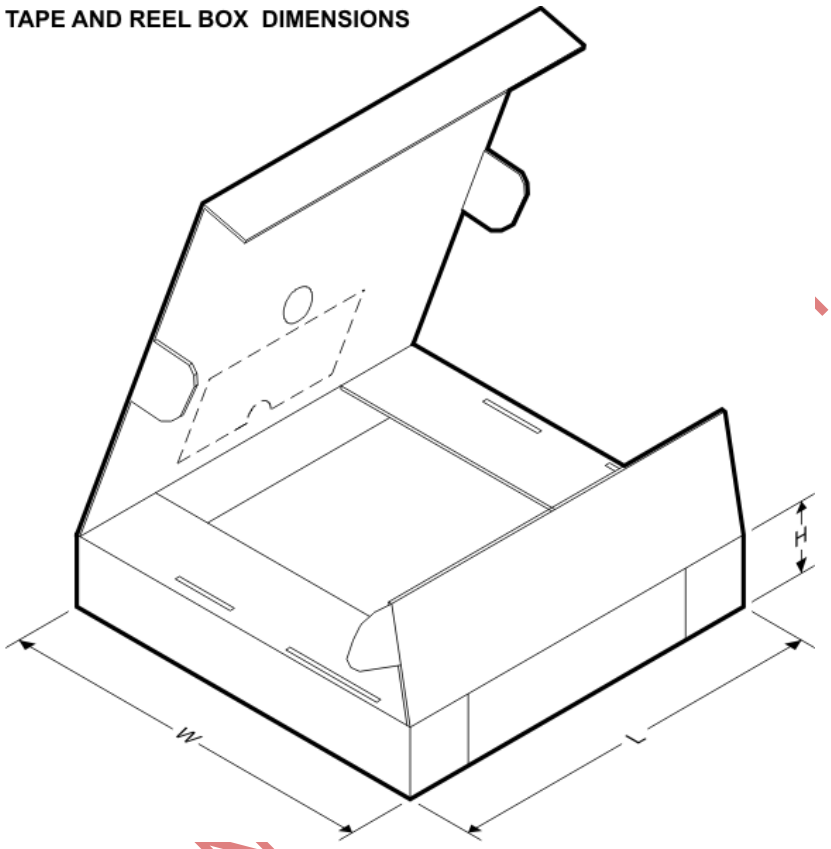


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CCD6805S	TSSOP	28	2500	330.0	16.5	6.90	10.20	1.60	12.00	16.0	Q1

图 **17-3** 内盒尺寸



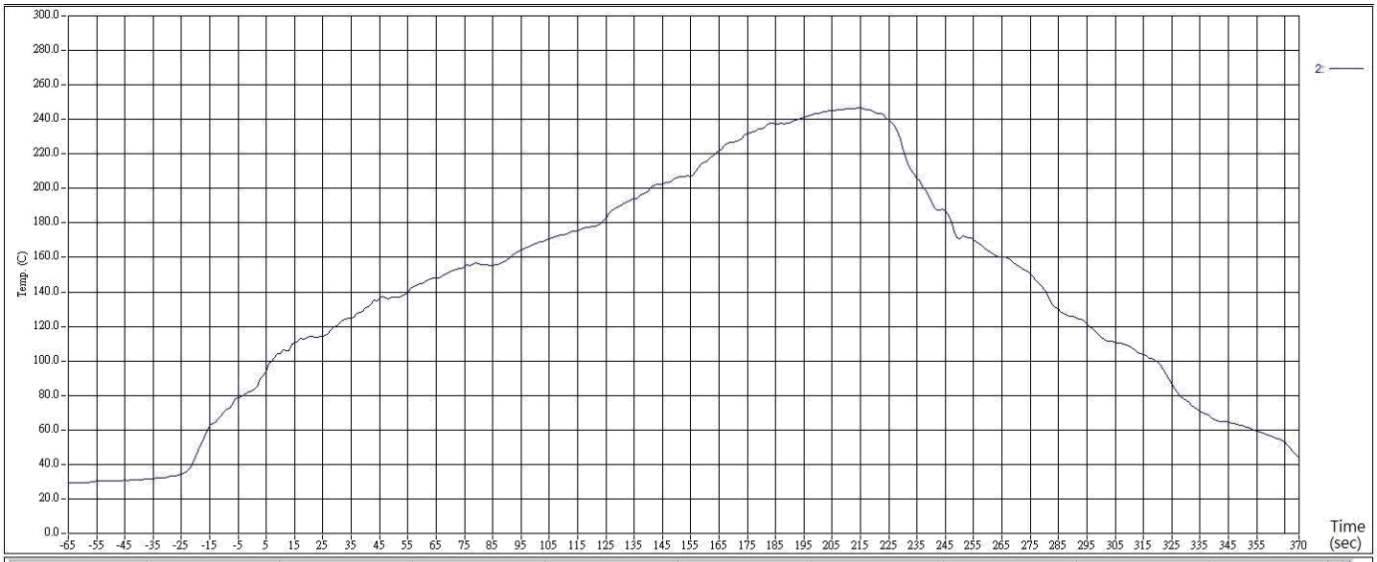
Device	Package Type	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	Eco Plan	MSL Level	MOQ
CCD6805S	TSSOP	28	2500	356.0	338.0	51.1	RoHS	MSL 3	2500

Marking：

CCD6805S Device Name
LINK-IC Producer
AAAAAA B YY WW

WW：Week-01;02;03…
YY：Year-25,26,27…
Fab Number
Lot Number

18. 焊接信息



	Ave Ramp up rate(T)	Holding Time	Peak Temp.	Liquidus Temp.	Time Above Temp.	Ave Cooling rate(T)			Result
Boundary	217.00-245.00 C	150.00-200.00 C	-------	217.00 C	240.00 C	245.00-217.00 C			
Range	0.00-3.00 (C/sec)	60.00-120.00 (sec)	245.00-250.00 (C)	60.00-150.00 (sec)	30.00-40.00 (sec)	6.00-0.00 (C/sec)			
sensor2	0.64	72.00	246.62	70.00	32.00	2.51			OK

19. 修订历史

表 **19-1** 文档版本历史

日期	版本	修改记录
25/8/20	V0.9	Initial Release
25/9/2	V0.94	Update first page, Marking information, Device List
25/9/5	V0.95	Update PVDD idle current, 384k plots, PKG information
25/9/25	V0.96	EC table add Smart Silent, direct AVDD data
25/9/29	V0.97	Change “Smart Sense Hiz mode” to “Smart Silent mode”, change “Direct Power efficiency mode” to “Direct ECO mode”
25/10/9	V0.98	Update application schematic

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