2x135W、4x66W 或 2.1 模式（2x66W + 1x135W）@1%失真数字输入 D 类音频放大器

1. 说明

CCD12076 是一款易于使用、高度集成、高性能、数字输入的 D 类音频放大器，内置高精度的 DAC 将接收的数字信号转换为模拟信号并放大输出。数字音频接口自适应 I2S 和 TDM 时钟频率，从而减少了 I2C 编程的需要。

这种大型高功率单芯片解决方案降低了整体系统解决方案的尺寸和成本。其数字音频接口非常灵活，支持 I2S、左对齐、右对齐和 TDM 4，TDM 8 数据格式。该芯片无需常用于数字信号通信外部的 MCLK 信号，这不仅减少了尺寸和引脚，还减少了 EMI 和可能的电路板耦合问题。

2. 优点和特性

- HBM ESD 分类等级 2
- CDM ESD 分类等级 C2A

➢ 音频输入
- Fs: 44.1 kHz, 48 kHz and 96 kHz
- I^2S, TDM 4 and 8

➢ 音频输出
- 4 通道负载 (BTL), 可选择的 2 通道负载 (PBTL)
- 480KHz and 2.1MHz FSW
- 4 x 66 W, 1% THDN, 25V, 4 Ω (BTL)
- 2 x 135 W, 1% THDN,25 V, 2 Ω (PBTL)
- 2 x 80 W, 1% THDN,25 V, 4 Ω (PBTL)
- 4 x 80 W, 10% THDN, 25 V, 4 Ω (BTL)
- 2 x160 W, 10% THDN, 25 V, 2 Ω (PBTL)
- 2 x 94 W, 10% THDN, 25 V, 4 Ω (PBTL)

➢ 14.4v，4 Ω时音频性能
- 效率 >90%
- 1W 时，THD+N < 0.03%
- 47μVRMS 输出噪声
- 90dB 串扰

➢ 高级负载诊断
- 输出开路和短路负载
- 输出到电源或接地短路
- 主机独立式操作

➢ 保护
- 输出短路保护
- 输出 DC 偏移保护
- 温度过高保护
- 欠压和过压保护

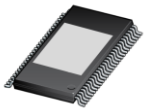
➢ 一般操作
- 4.5V 到 26.4V 电源电压
- 4 个 I2C 地址选择
- 过温自动调节
- 基于 THD+N 的可调失真防止烧喇叭
- 软静音功能
- 内置 PVDD 和 温度检测功能，通过 I2C 实时读取
- 无需 MCLK

3. 应用

- 蓝牙和 WIFI 无线音箱
- 条形音箱
- 家庭影院、低音炮
- 监听音箱
- 专业和公共广播（PA）扬声器

器件信息

器件编号	封装	封装尺寸（标称值）
CCD12076	SSOP EP (56)	18.41 mm × 7.49 mm



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4. 引脚配置与功能

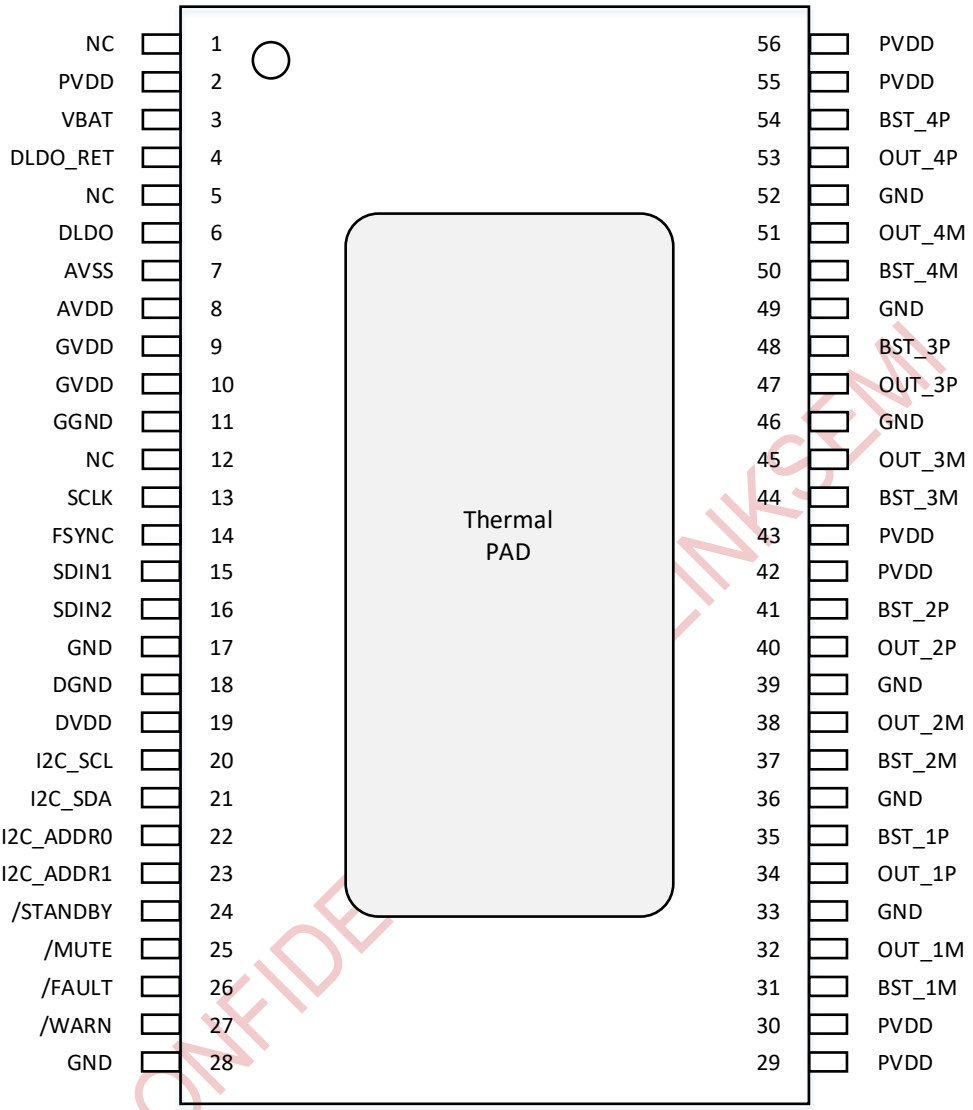


Figure 4-1 SSOP56-ep. Pad up, Top view

Table 4-1 Pin functions

引脚		描述
名称	编号	
NC	1、5、12	无需连接
PVDD	2、29、30、42、43、55、56	PVDD 电压输入。需要使用大容量电容和旁路电容
VBAT	3	电池电压输入
DLDO_RET	4	DLDO 旁路电容返回
DLDO	6	1.8V 稳压器输出。需连接一个 1μF 的电容，一端接 DLDO，另一端接 DLDO 返回端
AVSS	7	AVDD 旁路电容返回端

AVDD	8	电压调节器旁路。需连接一个 1μF 的电容，一端接 AVDD，另一端接 AVSS。
GVDD	9、10	从 VBAT 输入引脚派生的门极驱动电压调节器。需要连接一个 2.2 μF 的电容至地（GND），以提供稳定的电源并滤除高频噪声。
GND	11、17、18、28、33、36、39、46、49、52	接地
SCLK	13	音频数据位和串行时钟输入
FSYNC	14	音频帧时钟输入
SDIN1	15	TDM 数据输入或音频 I2S 通道 1 和 2 的数据输入
SDIN2	16	音频 I2S 通道 3 和 4 的数据输入
GND	17	接地
DVDD	19	3.3V 外部供电电压
I²C _SCL	20	I²C 时钟输入
I²C _SDA	21	I²C 数据输入和输出
I²C _ADDR0	22	I²C 地址引脚
I²C _ADDR1	23	
/STANDBY	24	启用低功耗待机状态（低电平有效），内部有 100 kΩ 的下拉电阻
/MUTE	25	静音设备输出（低电平有效），PWM 有 switching，内部有 100 kΩ 的下拉电阻
/FAULT	26	故障信号，低电平有效，开漏输出
/WARN	27	警告信号，低电平有效，开漏输出
BST_1M	31	用于高端栅极驱动器的自举电容连接引脚
OUT_1M	32	通道的负输出
OUT_1P	34	通道的正输出
BST_1P	35	用于高端栅极驱动器的自举电容连接引脚
BST_2M	37	用于高端驱动器的自举电容连接引脚
OUT_2M	38	通道的负输出
OUT_2P	40	通道的正输出
BST_2P	41	用于高端栅极驱动器的自举电容连接引脚
BST_3M	44	用于高端栅极驱动器的自举电容连接引脚
OUT_3M	45	通道的负输出
OUT_3P	47	通道的正输出
BST_3P	48	用于高端栅极驱动器的自举电容连接引脚
BST_4M	50	用于高端栅极驱动器的自举电容连接引脚
OUT_4M	51	通道的负输出
OUT_4P	53	通道的正输出
BST_4P	54	用于高端栅极驱动器的自举电容连接引脚
Thermal Pad	--	为设备提供电气和热连接。散热器应连接至地（GND）。

5. 绝对最大额定值

在自由空气操作温度范围内（除非另有说明），请参阅 (3)

		最小值	最大值	单位
PVDD, VBAT	相对于地（GND）的直流电源电压	-0.3	30	V
V_{RAMP}	供电电压上升速率：PVDD，VBAT		70	V/ms
VDD	相对于地（GND）的直流电源电压		VDD+0.5	V
I_{MAX}	每个引脚的最大电流（PVDD、VBAT、OUT_xP、OUT_xM、GND）		±8	A
V_{LOGIC}	逻辑引脚的输入电压（SCL、SDA、SDIN1、SDIN2、BCLK、LRCLK、/MUTE、/STANDBY、I2C_ADDRx）		VDD+0.5	V
V_{GND}	地（GND）引脚之间的最大电压	-0.3	+0.3	V
T_A	环境工作温度	-25	85	°C
T_{stg}	存储温度	-40	125	°C

(3) 超出绝对最大额定值范围运行可能导致设备永久损坏。绝对最大额定值并不意味着设备在这些条件或超出推荐工作条件所列的任何其他条件下能够正常运行。如果在推荐工作条件之外，但仍在绝对最大额定值范围内使用，设备可能无法完全正常工作，这可能会影响设备的可靠性、功能、性能，并缩短设备的使用寿命。

6. 推荐工作条件

			最小值	典型值	最大值	单位
PVDD	输出场效应晶体管（FET）的供电电压	相对于地	4.5		26.4	V
VBAT	电池供电电压输入	相对于地	4.5		18	V
VDD	直流逻辑电源	相对于地	3.0	3.3	3.6	V
T_A	环境温度		-40		85	°C
T_J	结温	需要进行充分的热设计	-40		150	°C
R_L	标称扬声器负载阻抗	BTL 模式	2	4		Ω
R_{PU_I2C}	SDA 和 SCL 引脚上的 I²C 上拉电阻			4.7		kΩ
C_{Bypass}	旁路引脚上的外部电容	引脚 2, 3, 6, 8, 19		1		μF
C_{GVDD}	GVDD 引脚上的外部电容	引脚 10		2.2		μF
C_{OUT}	输出引脚（OUT）到地（GND）的外部电容	由直流诊断定时设置的限制		1	2.2	μF
L_O	输出滤波电感	在 ISD 电流水平下的最小电感	1			μH

7. 静电等级

			值	单位
$V_{(ESD)}$	静电放电	人体模型（HBM），符合 ANSI/ESDA JEDEC JS-001 标准，所有引脚(4)	±2000	V
		充电器件模型（CDM），符合 JEDEC 标准 JESD22-C101，所有引脚(5)	±500	

(4) JEDEC 文件 JEP155 指出，500V 人体模型（HBM）允许在标准静电防护控制流程下安全进行生产制造。

(5) JEDEC 文件 JEP157 指出，250V 充电器件模型（CDM）允许在标准静电防护控制流程下安全进行生产制造

8. 热信息

热性能指标		CCD12076 (6)(7) SSOP EP (56) 56PINS	单位
$R_{\theta JA}$	结到环境的热阻	35	°C/W
$R_{\theta JC(top)}$	结到外壳（顶部）的热阻	0.4	°C/W
$R_{\theta JB}$	结到基板的热阻	15	°C/W
Ψ_{JT}	结到顶部的特性参数	0.2	°C/W
Ψ_{JB}	结到基板的特性参数	14	°C/W
$R_{\theta JC(bot)}$	结到外壳（底部）的热阻	-	°C/W

(6) JEDEC 标准四层 PCB

(7) 使用设备评估模块（EVM）布局和散热器测量的。该设备不建议在没有散热器的情况下使用。

9. 电气特性

测试条件（除非另有说明）：环境温度（TC）= 25°C，PVDD = VBAT = 14.4 V，VDD = 3.3 V，负载阻抗（RL）= 4 Ω，每通道输出功率（Pout）= 1 W，测试频率（f）= 1 kHz，开关频率（fSW）= 480 kHz，工作模式：桥接双线（BD）模式，滤波器：AES17 滤波器，I²C 设置：默认设置 LC 滤波器：10μH + 1μF，所列参数均在 XLINKSEMI CCD12076 评估模块（EVM）上测量。

参数		测试条件	最小值	典型值	最大值	单位
工作电流						
I_{PVDD_IDLE}	PVDD 空闲电流	所有通道播放，无音频输入		38		mA
I_{VBAT_IDLE}	VBAT 空闲电流	所有通道播放，无音频输入		37		mA
I_{PVDD_STBY}	PVDD 待机电流	/STANDBY 激活, VDD = 0 V		1		μA
V_{BAT_STBY}	VBAT 待机电流	/STANDBY 激活, VDD = 0 V		10		μA
I_{VDD}	VDD 供电电流	所有通道播放, 输入信号为–60dB		5		mA
输出电压						
P_{O_BTL}	每个通道的 BTL 输出功率	4 Ω, PVDD = 14.4 V, THD+N = 1%	21	24		W
		4 Ω, PVDD = 14.4 V, THD+N = 10%	25	28		
		2 Ω, PVDD = 14.4 V, THD+N = 1%	39	41		
		2 Ω, PVDD = 14.4 V, THD+N = 10%	43	47		
		4 Ω, PVDD = 25 V, THD+N = 1%	62	66		
		4 Ω, PVDD = 25 V, THD+N = 10%	70	80		
P_{O_PBTL}	每个通道的 PBTL 输出功率	2 Ω, PVDD = 14.4 V, THD+N = 1%	41	46		
		2 Ω, PVDD = 14.4 V, THD+N = 10%	50	56		
		2 Ω, PVDD = 25 V, THD+N = 1%	120	135		
		2 Ω, PVDD = 25 V, THD+N = 10%	140	165		
		4 Ω, PVDD = 25 V, THD+N = 1%	70	80		
		4 Ω, PVDD = 25 V, THD+N = 10%	79	89		
EFF_P	功率效率	4 个通道运行，每个通道输出功率为 25 W，负载阻抗为 4 Ω，PVDD = 14.4 V，环境温度（Tc）= 25°C，包括电感损耗		92		%
Rdson	场效应晶体管漏极到源极电阻	不包括键合线和封装电阻		65		mΩ
V_n	输出噪声电压	零输入，A 加权，增益水平 1, PVDD = 14.4 V		42		μV
		零输入，A 加权，增益水平 2, PVDD = 14.4 V		47		
		零输入，A 加权，增益水平 3, PVDD = 18 V		47		
		零输入，A 加权，增益水平 4, PVDD = 25 V		55		
GAIN	峰值输出电压/每分贝全标度	Gain level 1, Register 0x01, bit 1-0 = 00		7.5		V/FS
		Gain level 2, Register 0x01, bit 1-0 = 01		15		
		Gain level 3, Register 0x01, bit 1-0 = 10		21		
		Gain level 4, Register 0x01, bit 1-0 = 11		29		
Crosstalk	频道串扰	PVDD = 14.4 Vdc + 1 V_{RMS}, f = 1 kHz		-90		dB
PSRR	电源抑制比	PVDD = 14.4 Vdc + 1 V_{RMS}, f = 1 kHz		-75		dB
THD+N	总谐波失真加噪声			0.02	0.05	%
G_{VAR}	增益变化	All gain levels	-0.5	0	0.5	dB
G_{CH}	通道间增益变化		-0.5	0	0.5	dB
线路输出						
V_O	线路输出电压	0dB 输入，线路输出（LO）模式，增益级		5.5		Vrms

		别 1				
		0dB 输入，线路输出（LO）模式，增益级别 2		10.5		
I2C/I2S 数字 IO 引脚						
V_{IH}	输入逻辑高电平		1.7			V
V_{IL}	输入逻辑低电平				0.95	V
I_{IH}	输入逻辑高电平电流	VI = DVDD			15	μA
I_{IL}	输入逻辑低电平电流	VI = 0			-15	μA
过压保护						
V_{PVDD_OV}	PVDD 过压保护		27	27.8	28.8	V
$V_{PVDD\_OV\_HYS}$	PVDD 过压保护迟滞			1.1		V
V_{VBAT_OV}	VBAT 过压保护		18.8	20	21.2	V
$V_{VBAT\_OV\_HYS}$	VBAT 过压保护迟滞			0.7		V
欠压保护						
$VBAT_{UV}$	VBAT 欠压关闭			4	4.4	V
$VBAT_{UV\_HYS}$	VBAT 欠压关闭滞后			0.4		V
$PVDD_{UV}$	PVDD 欠压关闭			4	4.4	V
$PVDD_{UV\_HYS}$	PVDD 欠压关闭迟滞			0.3		V
旁路电压						
V_{GVDD}	栅极驱动旁路引脚电压		4.9	5.15	5.4	V
V_{AVDD}	模拟旁路引脚电压		4.9	5.15	5.4	V
V_{DLDO}	DLDO 旁路引脚电压		1.62	1.8	1.98	V
上电复位						
V_{POR}	VDD 电压用于上电复位			2.1		V
V_{POR_HYS}	VDD POR 恢复迟滞电压			0.5		V
过温保护						
OTW(i)	通道过温警告			150		°C
OTSD(i)	通道过温关闭			175		°C
OTW	全局结温过温警告			130		°C
OTSD	全局结温过温关闭			160		°C
OT_{HYS}	过温迟滞			15		°C
负载过流保护						
I_{SD}	过流关断	OC 等级 1，任何短路至电源、地或其他通道的过流保护。		7.5		A
		OC 等级 2，任何短路至电源、地或其他通道的过流保护。		10		A
咔嗒声和爆音						
V_{CP}	咔嗒声和爆音输出电压	ITU-R 2kHz 滤波器，高阻抗/静音到播放，播放到静音/高阻抗		3		mV
直流偏移						
V_{OFFSET}	输出偏移电压			1	2	mV
直流检测						

DC_{FAULT}	输出直流故障保护			2		V
削波						
$t_{DELAY\_CLIPDET}$	检测到输出削波时的信号延迟				20	μs
负载诊断						
S2P	检测输出引脚（OUT）到 PVDD 短路的最大电阻				3000	Ω
S2G	检测输出引脚（OUT）到地短路的最大电阻				200	Ω
SL	短路负载检测容差	其他通道处于高阻态		0.5		Ω
OL	开路负载（负载断开）	其他通道处于高阻态		32		Ω
T_{DC_DIAG}	直流诊断时间	4 个通道无故障并联运行		175		ms
T_{LINE_DIAG}	线路输出诊断时间	1 个通道激活		42		ms

10. 主要电气参数的典型曲线

环境温度（Tc）= 25°C，数字电源电压（DVDD）= 3.3 V，电池电压（VBAT）= PVDD = 14.4 V，负载阻抗（RL）= 4 Ω，输入信号频率（FIN）= 1 kHz，采样频率（fs）= 48 kHz，开关频率（FSW）= 480 kHz，输出配置：桥接双线（BTL）模式，滤波器：AES17 滤波器，LC 滤波器：10μH + 1μF，以上曲线是在 XLINKSEMI CCD12076 评估模块（EVM）上测量得到的。

480K BTL

Figure 10-1 THD+N vs Power
PVDD=14.4V, 2ohm/4ohm. FSW = 480KHz, BTL

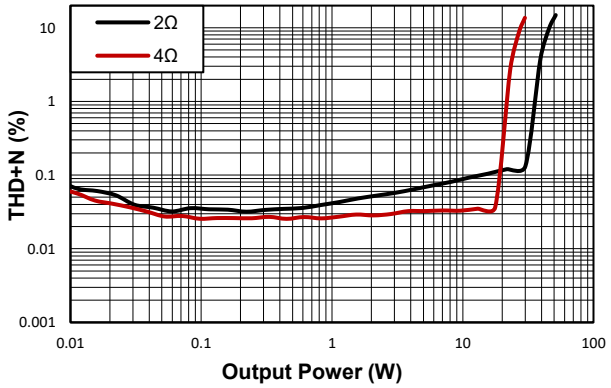


Figure 10-2 THD+N vs Frequency
PVDD=14.4V, 2ohm/4ohm, FSW = 480KHz, BTL

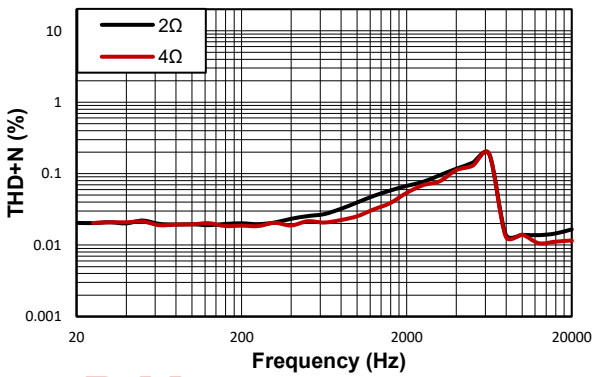


Figure 10-3 Output Power vs Supply Voltage
PVDD=5-25V, 4ohm, FSW = 480KHz, BTL

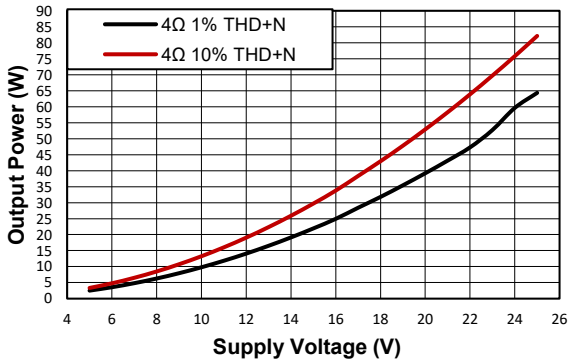


Figure 10-4 Efficiency vs Output Power
PVDD=14.4V, 4ohm, FSW = 480KHz, BTL

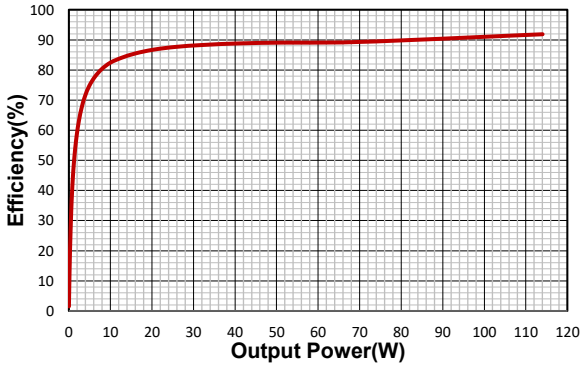


Figure 10-5 Efficiency vs Output Power
PVDD=14.4V, 4ohm, FSW = 480KHz, BTL

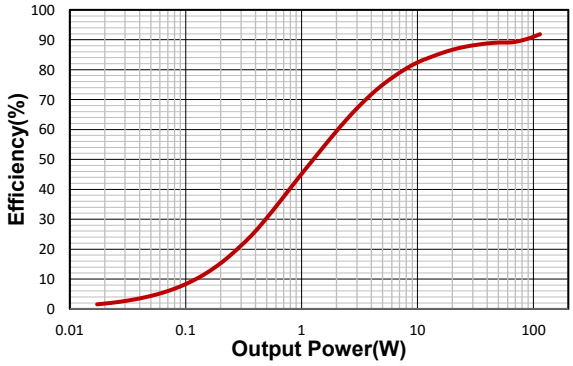
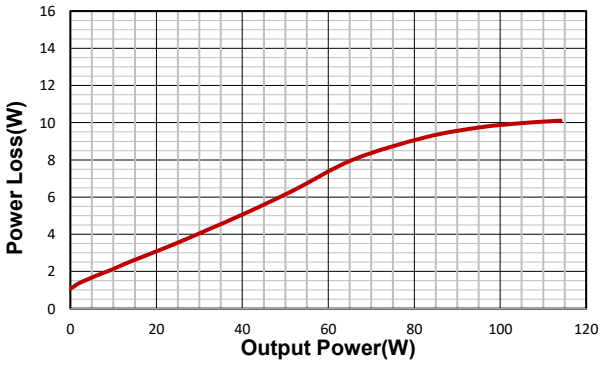


Figure 10-6 Power Loss vs Output Voltage
PVDD=14.4V, 4ohm, FSW = 480KHz, BTL



480K BTL

Figure 10-7 Efficiency vs Output Power
PVDD=14.4V, 2ohm, FSW = 480KHz, BTL

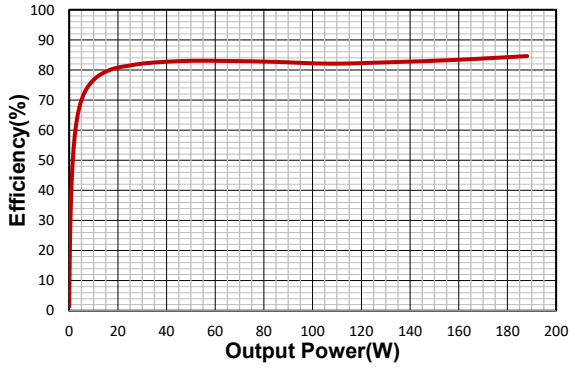


Figure 10-8 Efficiency vs Output Power
PVDD=14.4V, 2ohm, FSW = 480KHz, BTL

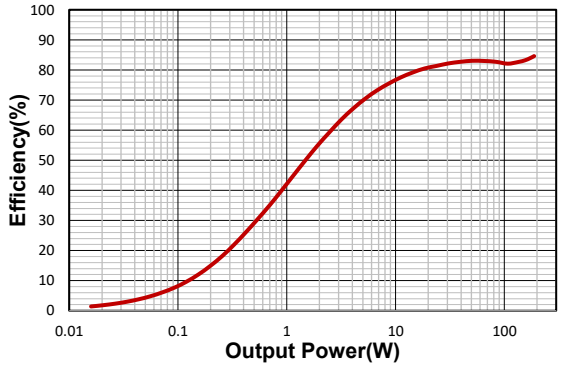


Figure 10-9 Power Loss vs Output Power
PVDD=14.4V, 2ohm, FSW = 480KHz, BTL

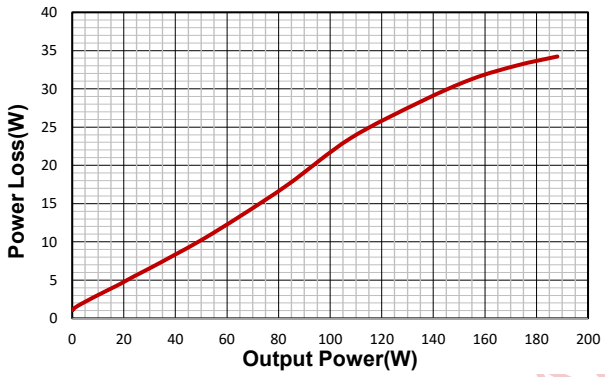


Figure 10-10 PVDD IDLE
PVDD=5-25V, 4ohm, FSW = 480KHz, BTL

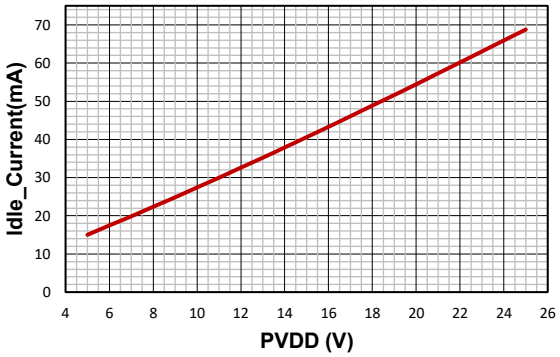


Figure 10-11 VBAT IDLE
PVDD=5-25V, 4ohm, FSW = 480KHz, BTL

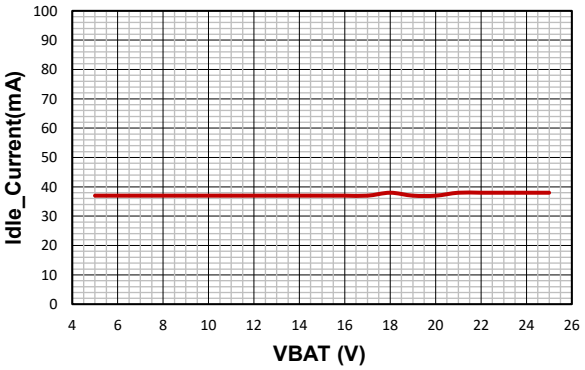
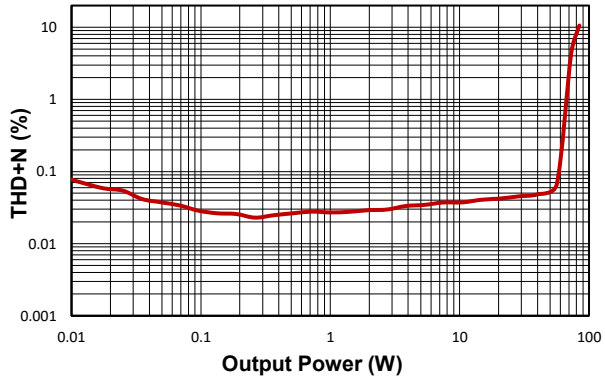


Figure 10-12 THD+N vs Power
PVDD=25V, 4ohm, FSW = 480kHz, BTL



480K BTL

Figure 10-13 THD+N vs Frequency
PVDD=25V, 4ohm, FSW = 480kHz, BTL

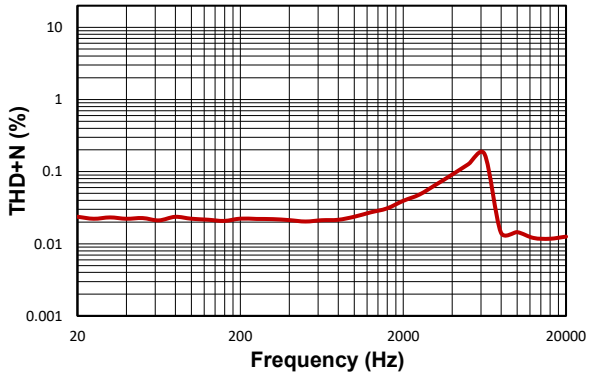


Figure 10-14 Efficiency vs Output Power
PVDD=25V, 4ohm, FSW = 480KHz, BTL

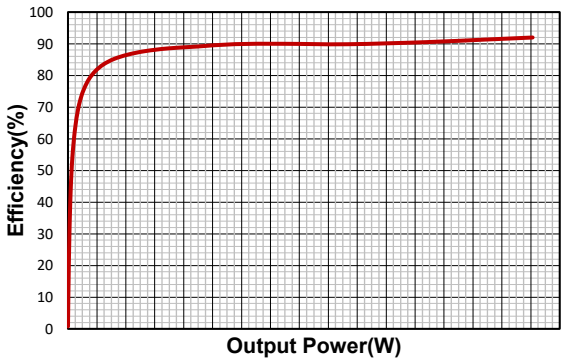


Figure 10-15 Efficiency vs Output Power
PVDD=25V, 4ohm, FSW = 480KHz, BTL

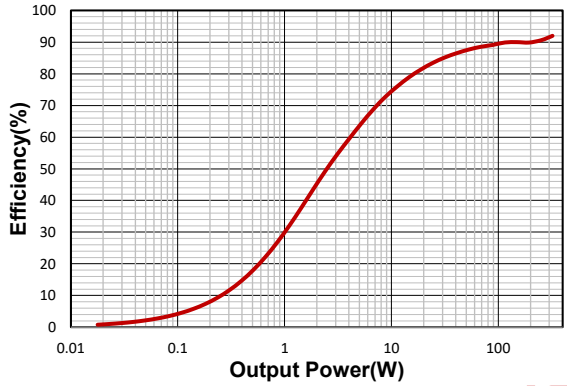


Figure 10-16 Power Loss vs Output Power
PVDD=25V, 4ohm, FSW = 480KHz, BTL

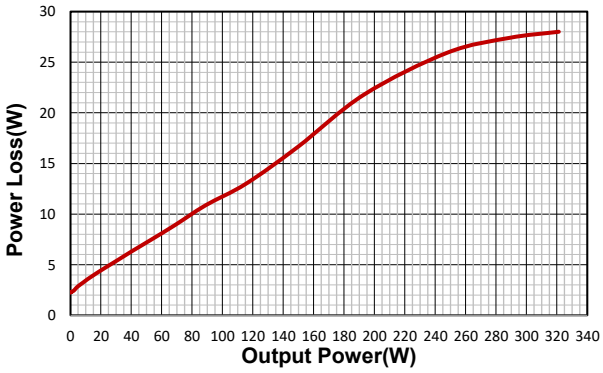


Figure 10-17 THD+N vs Power
PVDD=14.4V, 2ohm, FSW = 480KHz, PBTL

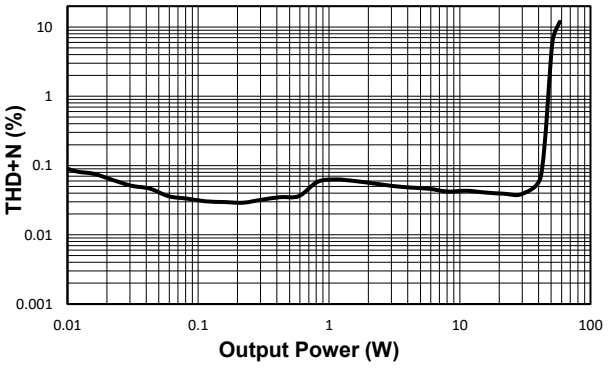
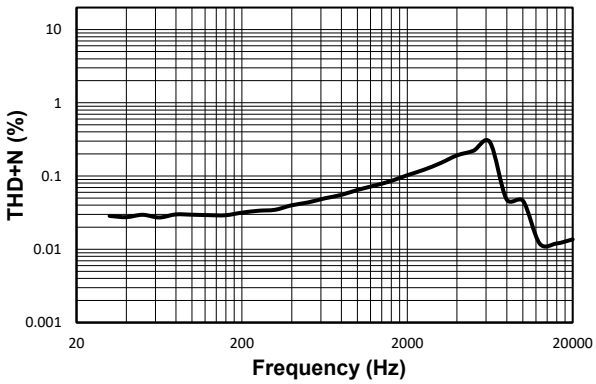


Figure 10-18 THD+N vs Frequency
PVDD=14.4V, 2ohm, FSW = 480KMHz, PBTL



480K BTL

Figure 10-19 Output Power vs Supply Voltage
PVDD=5-25V, 2ohm, FSW = 480KHz, PBTL

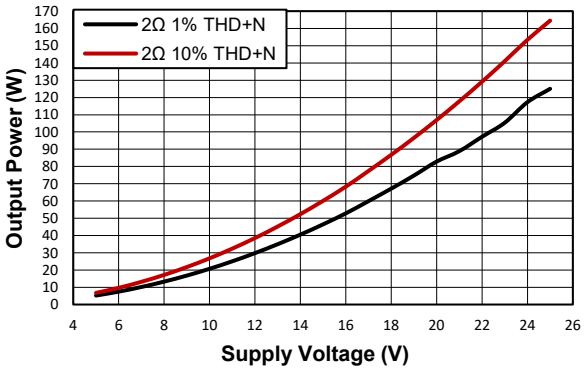
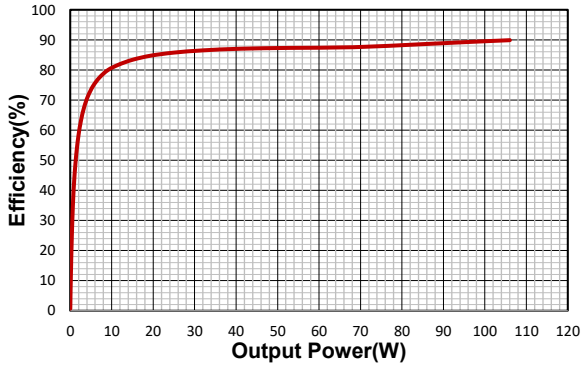


Figure 10-20 Efficiency vs Output Power
PVDD=14.4V, 2ohm, FSW = 480KHz, PBTL



480K PBTL

Figure 10-21 Efficiency vs Output Power
PVDD=14.4V, 2ohm, FSW = 480KHz, PBTL

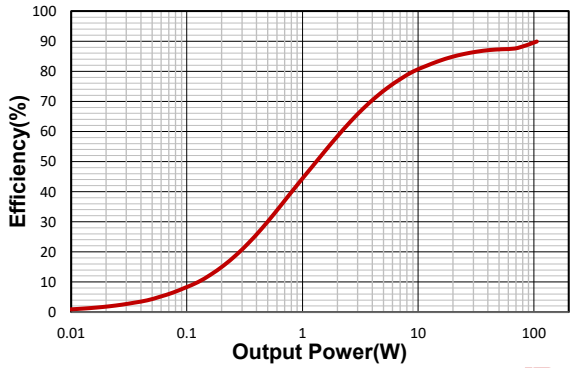


Figure 10-22 Power Loss vs Output Power
PVDD=14.4V, 2ohm, FSW = 480KHz, PBTL

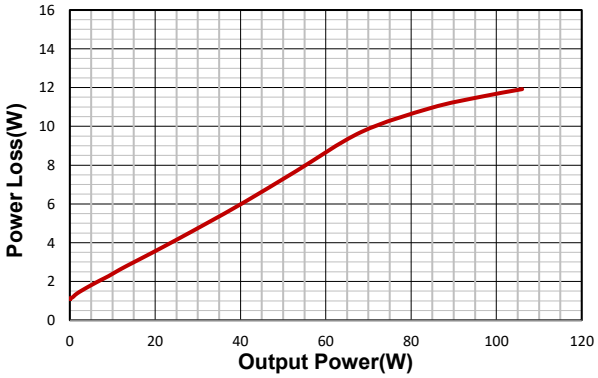


Figure 10-23 THD+N vs Power
PVDD=25V, 2ohm, FSW = 480KHz, PBTL

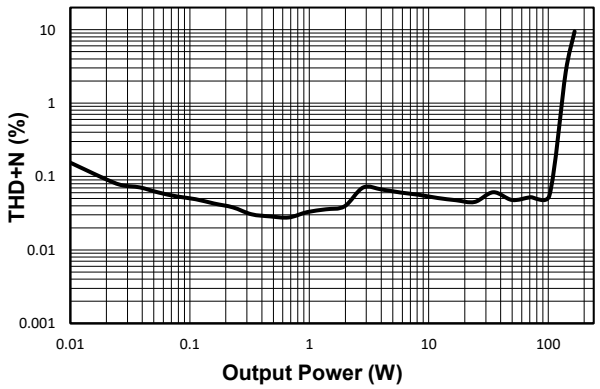
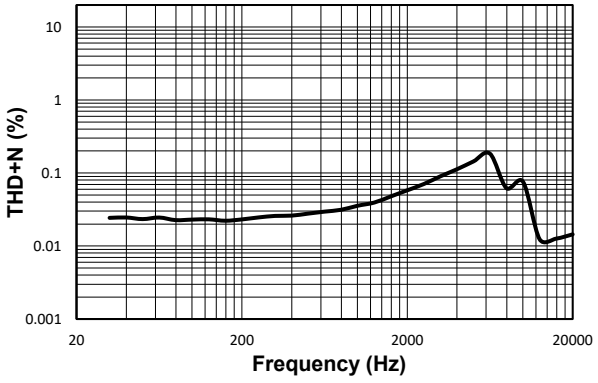


Figure 10-24 THD+N vs Frequency
PVDD=25V, 2ohm, FSW = 480KHz, PBTL



480K PBTL

Figure 10-25 Efficiency vs Output Power
PVDD=25V, 2ohm, FSW = 480KHz, PBTL

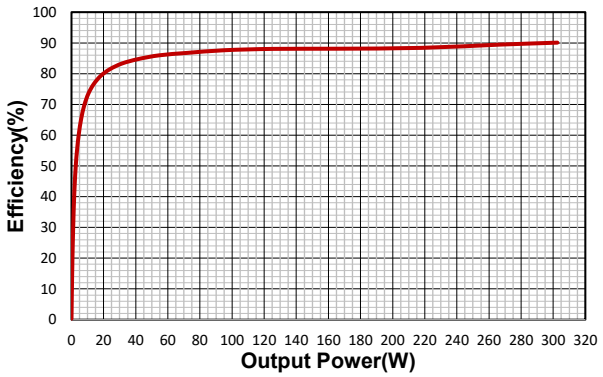


Figure 10-26 Efficiency vs Output Power
PVDD=25V, 2ohm, FSW = 480KHz, PBTL

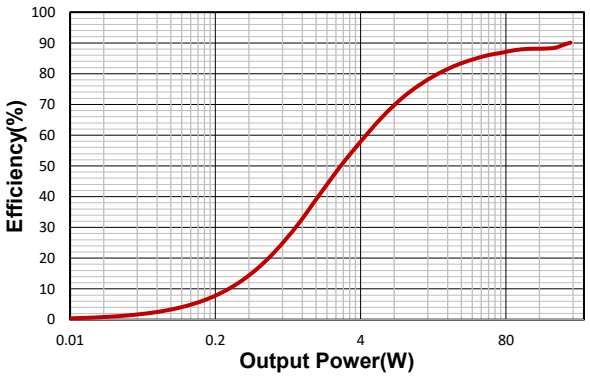


Figure 10-27 Power Loss vs Output Power
PVDD=25V, 2ohm, FSW = 480KHz, PBTL

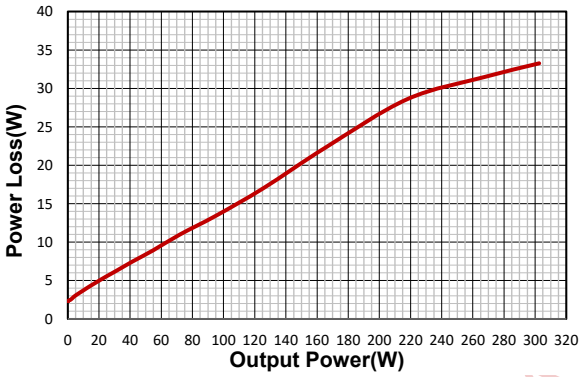


Figure 10-28 THD+N vs Power
PVDD=25V, 4ohm, FSW = 480KHz, PBTL

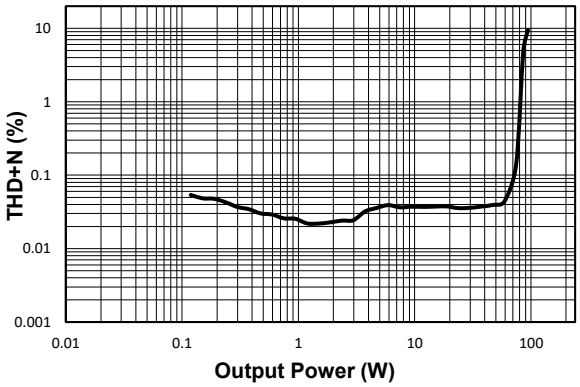
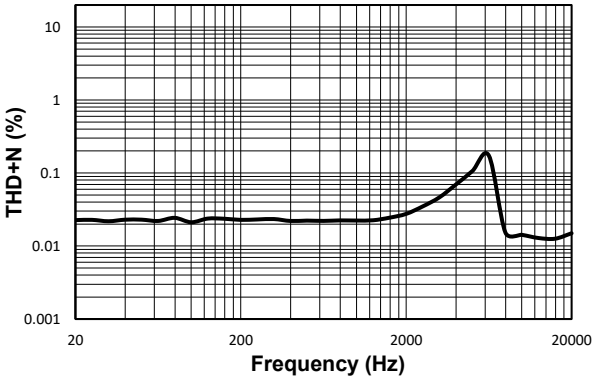


Figure 10-29 THD+N vs Frequency
PVDD=25V, 4ohm, FSW = 480KHz, PBTL



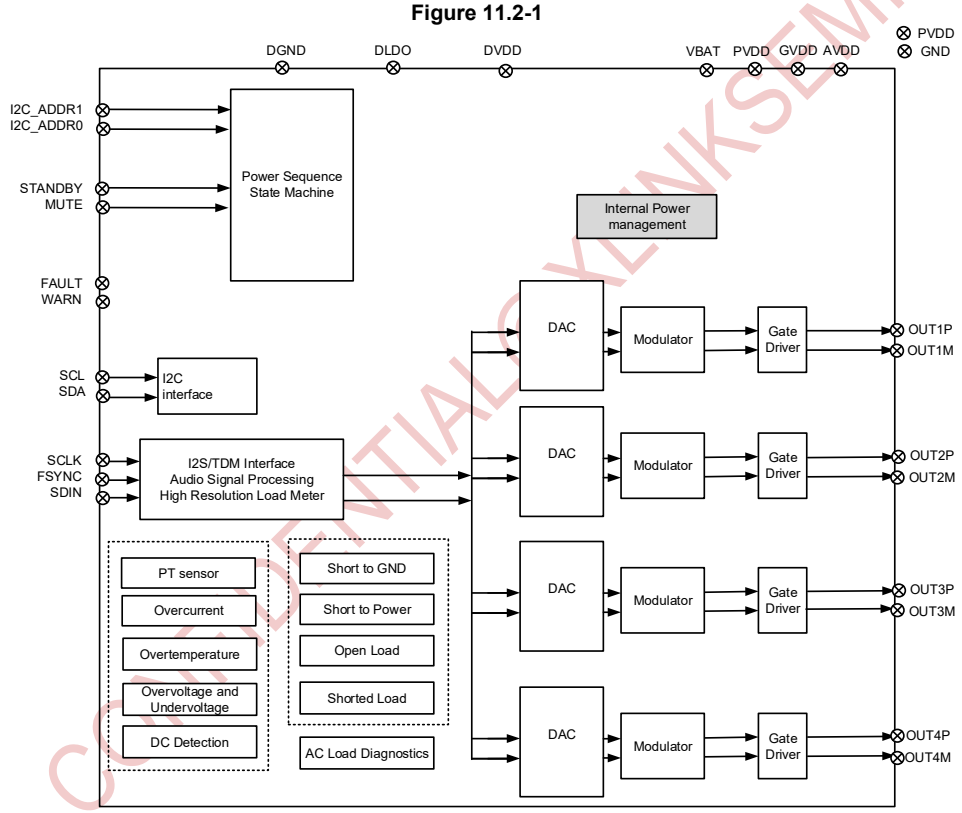
11. 详细描述

11.1. 总览

CCD12076 是一款 4 通道数字输入 D 类音频放大器。它是一款具有高环路带宽的全闭环放大器，并且能够灵活地在 AM 频段以上或以下进行开关切换。该放大器提供高效率、低噪声以及无咔嗒声和爆音的性能，使其非常适合用于现代信息娱乐系统。

11.2 功能模块图

Figure 11.2-1



11.3 串行音频接口

11.3.1 串行音频端口

CCD12076 支持标准的 I2S 格式或 TDM 格式。I2S 总线需要 4 条线：数据时钟（SCLK）、帧同步时钟（FSYNC）以及数据线（SDIN1 和 SDIN2）。

对于 I2S、TDM4 和 TDM8，串行音频端口可以通过寄存器 0x03 轻松配置。

音频接口	时钟等级	最大时钟等级
FSYNC	44.1K, 48K, 96K	96K
SCLK	64 x FSYNC (16-32 bit data/ 32 bit length), 128 x FSYNC (16-32 bit data/ 32 bit length), 256 x FSYNC (16-32 bit data/ 32 bit length)	12.288MHz

Table 11.3.1-1

11.3.2 I²S 模式

在这种模式下，FSYNC 时钟用于同步左右声道数据线的传输。在四通道应用中，需要两条数据线。SCLK 在 FSYNC 的下降沿进行同步，因此数据在 SCLK 的上升沿有效。

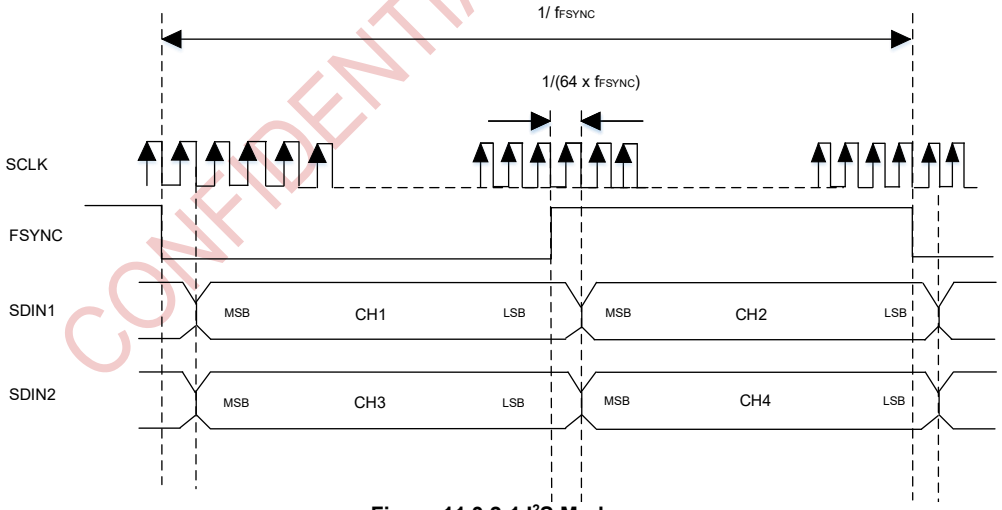


Figure 11.3.2-1 I²S Mode

11.3.3 TDM 模式

TDM 支持 4 通道和 8 通道。在 TDM4 模式下，SCLK 是 FSYNC 的 128 倍；在 TDM8 模式下，SCLK 是 FSYNC 的 256 倍。在 TDM 模式下，SDIN1 用于音频数据，SDIN2 可以接地或与 SDIN1 引脚相连。

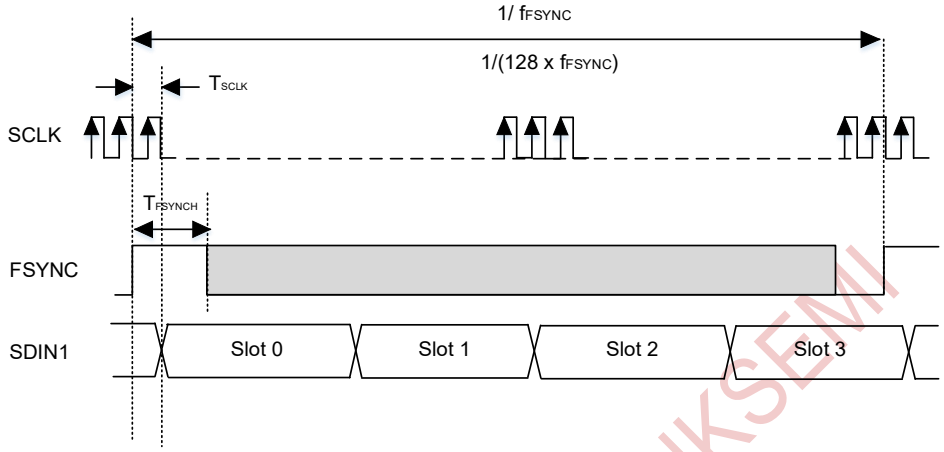


Figure 11.3.3-1 TDM4 Mode

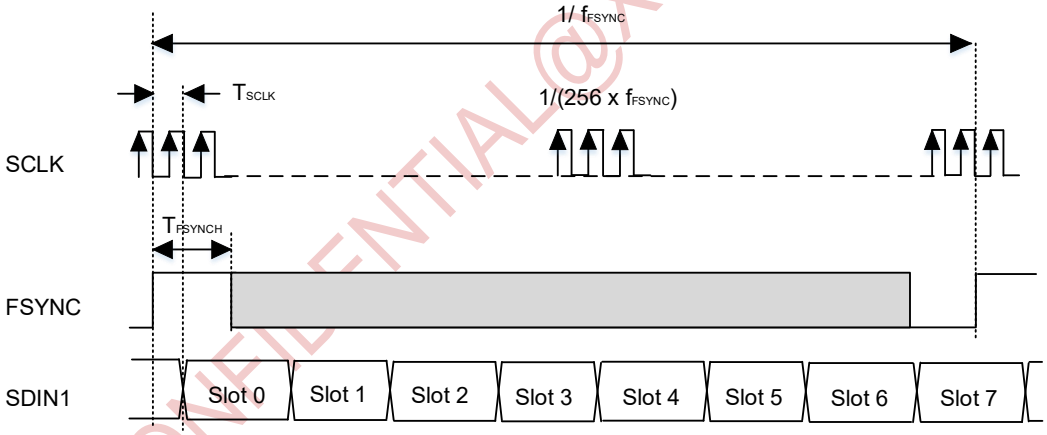


Figure 11.3.3-2 TDM8 Mode

Tabel 11.3.3-1 TDM Channel Selection

寄存器配置		TDM8 通道槽							
0x03 BIT 5	0x03 BIT 3	1	2	3	4	5	6	7	8
0	0	CH1	CH2	CH3	CH4	-	-	-	-
1	0	-	-	-	-	CH1	CH2	CH3	CH4
0	1	CH3	CH4	CH1	CH2	-	-	-	-
1	1	-	-	-	-	CH3	CH4	CH1	CH2

Tabel 11.3.3-2 TDM Channel Selection in PBTL Mode

寄存器配置			TDM8 通道槽							
0x03 BIT 5	0x03 BIT 3	0x21 BIT 6	1	2	3	4	5	6	7	8
0	0	0	PBTL CH1/2	-	PBTL CH3/4	-	-	-	-	-
1	0	0	-	-	-	-	PBTL CH1/2	-	PBTL CH3/4	-
0	0	1	-	PBTL CH1/2	-	PBTL CH3/4	-	-	-	-
1	0	1	-	-	-	-	-	PBTL CH1/2	-	PBTL CH3/4
0	1	0	PBTL CH3/4	-	PBTL CH1/2	-	-	-	-	-
1	1	0	-	-	-	-	PBTL CH3/4	-	PBTL CH1/2-	-
0	1	1	-	PBTL CH3/4	-	PBTL CH1/2	-	-	-	-
1	1	1	-	-	-	-	-	PBTL CH3/4	-	PBTL CH1/2

11.3.4 音频接口时序

音频接口时序		最小值	典型值	最大值	单位
Fsclk	SCLK(bit clock) frequency			24.576	MHz
Tsclk	SCLK period	41			ns
Tsclk_duty	SCLK duty cycle	45	50	55	%
Tsclkh	SCLK high time	16			ns
Tsclkl	SCLK low time	16			ns
Tds	SDIN setup time before SCLK rising edge	8			ns
Tdh	SDIN hold time after SCLK rising edge	8			ns
Trise/fall	SCLK rising and fall time			5	ns
Tfsynch	FSYNC high time	1 Tsclk			ns
Tfsyncs	FSYNC setup time	8			ns
Tfsynchd	FSYNC hold time	8			ns
Ci	Input capacitance, SLCK, FSYNC, SDIN1, SDIN2			10	pf

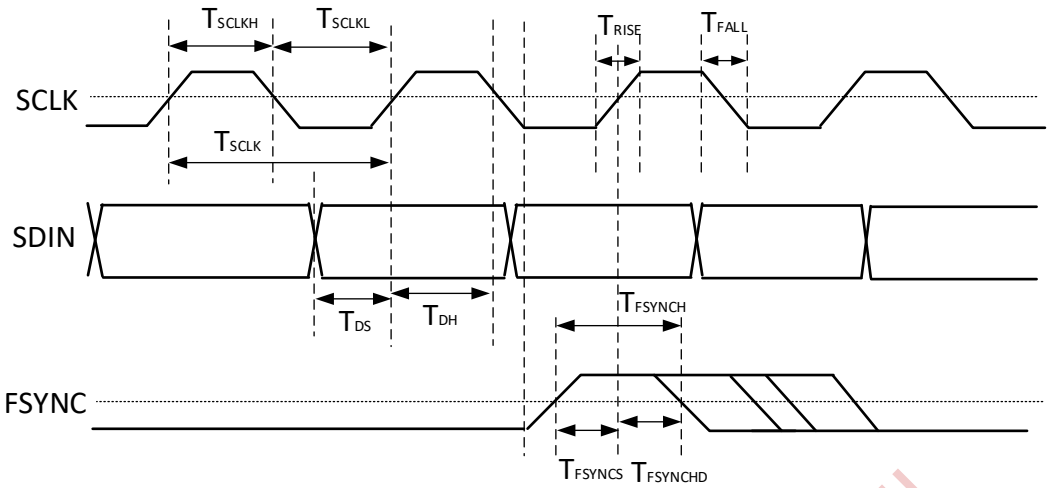


Figure 11.3.4-1 Audio interface timing

11.3.5 群延迟

在 CCD12076 中，群延迟随采样频率 Fs 变化，可以通过寄存器 0x03 进行配置，以下是所有配置下的典型值：

Table 11.3.5-1

输入采样频率 **(Fs)**	群延迟
44.1 KHz	500us
48 KHz	500us
96 KHz	104us

12. I²C 串行通信总线

该设备通过 I²C 总线与主机通信，典型的 I²C 时序图如下所示。

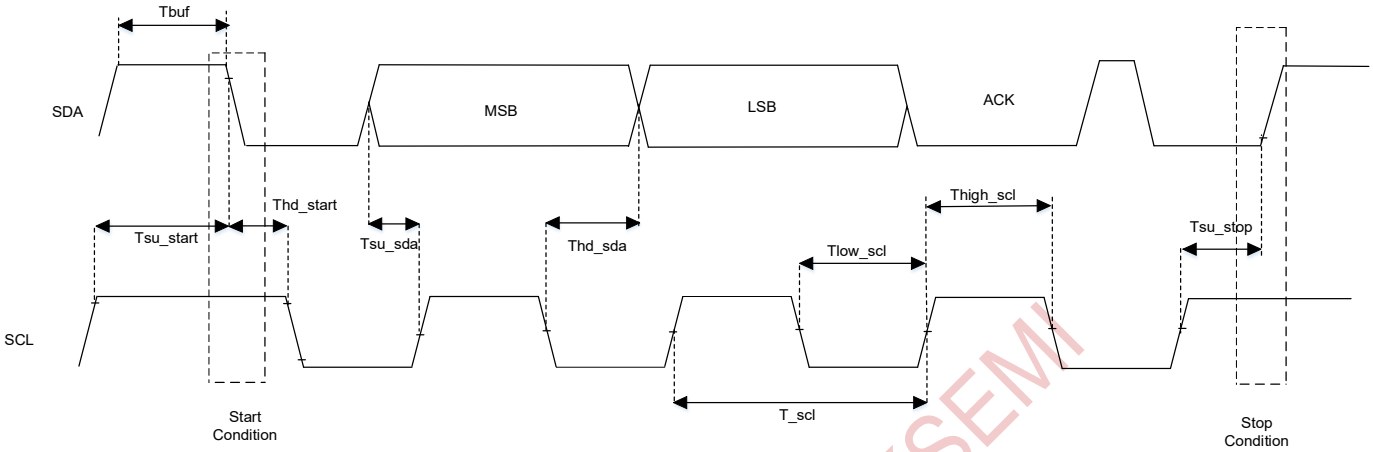


Figure 12-1 I²C Timing

Table 12-1 I²C Timing

I²C timing					
Fscl	I²C communication speed			400	KHz
Tbuf	Bus free time between stop and start	1.3			us
Tlow_scl	SCL low period	1.3			us
Thigh_scl	SCL high period	0.6			us
Tsu_start	Startup setup time	0.6			us
Thd_start	Startup hold time	0.6			us
Tsu_sda	SDA setup time	0.1			us
Thd_sda	SDA hold time	0.1			us
Tfall	Falling time			0.3	us
Trise	Rising time			0.3	us
Tsu_stop	Stop condition setup time	0.6			us

CCD12076 设备提供了 4 种地址设置选项：

描述	**I²C ADDR1**	**I²C ADDR0**	**Pull down config**	**I²C Write**	**I²C Read**
Device 1	0	0	0: Strong pull down (0-2.2Kohm)	0xD4	0xD5
Device 2	0	1		0xD6	0xD7
Device 3	1	0		0xD8	0xD9
Device 4	1	1		0xDA	0xDB

13. 负载诊断

CCD12076 设备为用户提供了精准的直流诊断功能，用于检测扬声器和高音喇叭应用中的任何异常情况。直流诊断会在 D 类放大器输出级准备切换之前每次进行。这种诊断技术集成了尖峰滤波功能，因此在嘈杂环境下（例如继电器切换、电磁干扰或诊断测试期间的干扰）具有很高的抗干扰能力。诊断功能不依赖于音频输入时钟，并且设计为所有通道并行运行。

13.1 直流负载诊断

DC DIAG Category	描述	特性
S2P	输出短路至电池	默认启用 所有通道并行运行
S2G	输出短路至接地	默认启用 所有通道并行运行
SL	短路负载	阈值可通过 I²C 调节 默认启用 所有通道并行运行
Normal Load	负载电阻在限定范围内	默认启用 所有通道并行运行
OL	开路负载表示负载已断开	默认启用
Lineout Load	负载电阻高于正常负载，但低于线路输出模式阈值（典型值为 12kΩ）。	默认禁用

14. 保护与监控

该设备集成了以下保护机制：

类别	引脚状态	行为	恢复到切换状态（假设故障已被排除）
DC offset	/FAULT 低电平有效	故障通道高阻态	锁存故障；通过 I²C 写入清除
OC	/FAULT 低电平有效	故障通道高阻态	锁存故障；通过 I²C 写入清除
Channel OTSD	/FAULT 低电平有效	故障通道高阻态	自动恢复或通过 I²C 实现相反操作。
UV/OV	/FAULT 低电平有效	所有通道高阻态	自动恢复
Global OTSD	/FAULT 低电平有效	所有通道高阻态	自动恢复或通过 I²C 实现相反操作。
CLK Fault	/FAULT 低电平有效	所有通道高阻态	自动恢复
Global OTW	/WARN 低电平有效	无变化	无
Channel OTW	/WARN 低电平有效	无变化	无
Clipping	/WARN 低电平有效	无变化	通过 I²C 实现锁存或非锁存。
POR	/WARN 低电平有效	无	通过 I²C 写入清除。

14.1 直流偏移检测器

直流偏移检测器用于保护扬声器免受放大器输出端可能出现的大直流偏移电压的损害。如果检测到的直流偏移超过设定阈值，设备会进入高阻态（HIZ），/FAULT 引脚会被拉低，并且可以通过 I²C 读取故障状态。这种保护机制通过高通滤波器来区分低频音频信号和直流偏移，确保只有在直流偏移超出安全范围时才会触发保护。.

14.2 削波检测器

该设备在运行过程中能够检测输出信号的削波现象。削波警告会报告到寄存器中，并且可以通过 I²C 清除。削波警告可以配置为锁存（latched）或非锁存（non-latched）模式。当输出信号发生削波时，/WARN 引脚会被拉低。

14.3 过电保护(OV)

当发生过电压事件时，设备进入高阻态（HIZ）以安全运行，/FAULT 引脚被拉低，且可以通过 I2C 读取故障状态。

14.4 过压保护(UV)

设备具备欠压保护功能。当检测到的电压低于欠压阈值（UV）时，设备会进入高阻态（HIZ），以防止因欠压导致的误操作。此时，/FAULT 引脚会被拉低，表明设备处于故障状态。用户可以通过 I2C 接口读取故障状态，以便进一步诊断和处理。

14.5 上电复位 (POR)

当欠压事件发生时，设备会发出欠压警告（Under Voltage，UV）。此时，数字核心的电压低于欠压复位（Power-On Reset，POR）阈值，所有寄存器都会重置为默认值。每次设备初始化或上电时，都会生成欠压警告，以便用户记录设备经历欠压条件的情况。建议清除相应的位，以使/FAULT 引脚恢复正常状态。

14.6 过流关断 (OCSD)

该设备集成了针对输出通道短路至电源或地的保护机制。它通过检测峰值电流，并在峰值电流超过过流阈值（OC）时关闭相应通道来实现保护。过流通道会被设置为高阻态（HIZ），/FAULT 引脚会被拉低，并且可以通过 I²C 读取故障状态。用户可以通过运行直流诊断（DC diagnostics）来确定短路类型（例如电源短路 S2P、对地短路 S2G 或负载短路 SL）。

14.7 全局过温警告和通道过温警告 (OTW)

设备实现了全局过温警告和通道过温警告。全局过温警告会影响所有通道，而通道过温警告仅对受影响的通道采取措施。全局过温警告具有 4 个可调节的级别。如果全局温度或通道温度超过过温警告（OTW）阈值，/WARN 引脚会被拉低。用户可以通过 I²C 屏蔽警告事件并清除警告。

14.8 过温关断(OTSD)

设备实现了全局过温关断保护和通道过温关断保护。全局过温关断（OTSD）会关闭所有通道，而通道过温关断仅对受影响的通道采取措施。设备提供自动恢复功能，在这种情况下，当温度低于过温关断恢复阈值时，设备将恢复到播放状态。

15. 设备启动和关闭顺序

该设备需要 3 个外部电源：VBAT、PVDD 和 DVDD。

VBAT 可以直接连接到 4.5V 至 18V 的电池。为了获得更好的性能，电池电压应超过 7V。VBAT 是为功率场效应晶体管（Power-FET）栅极驱动器供电的电源。PVDD 是功率场效应晶体管的供电电源，它会汲取高电流，可以连接到电池或连接到高达 26.4V 的升压系统电源轨。DVDD 是数字 I/O 电源。

启动顺序：

1. 配置 Addr0 和 Addr1 引脚以设置 I²C 地址。
2. 上电 VBAT、PVDD 和 DVDD，PVDD、VBAT 和 DVDD 之间没有严格的时序要求。
3. 在电源稳定后拉高/STANDBY 引脚，此操作必须在发送 I²C 命令之前完成。
4. 建议在发送 I²C 播放命令之前准备好 I2S/TDM 信号。
5. 在/STANDBY 引脚被拉高后，I²C 接口可以访问。

关闭顺序：

1. 将/STANDBY 引脚配置为低电平。
2. 至少等待 5 毫秒。
3. 关闭 PVDD、DVDD 和 VBAT。

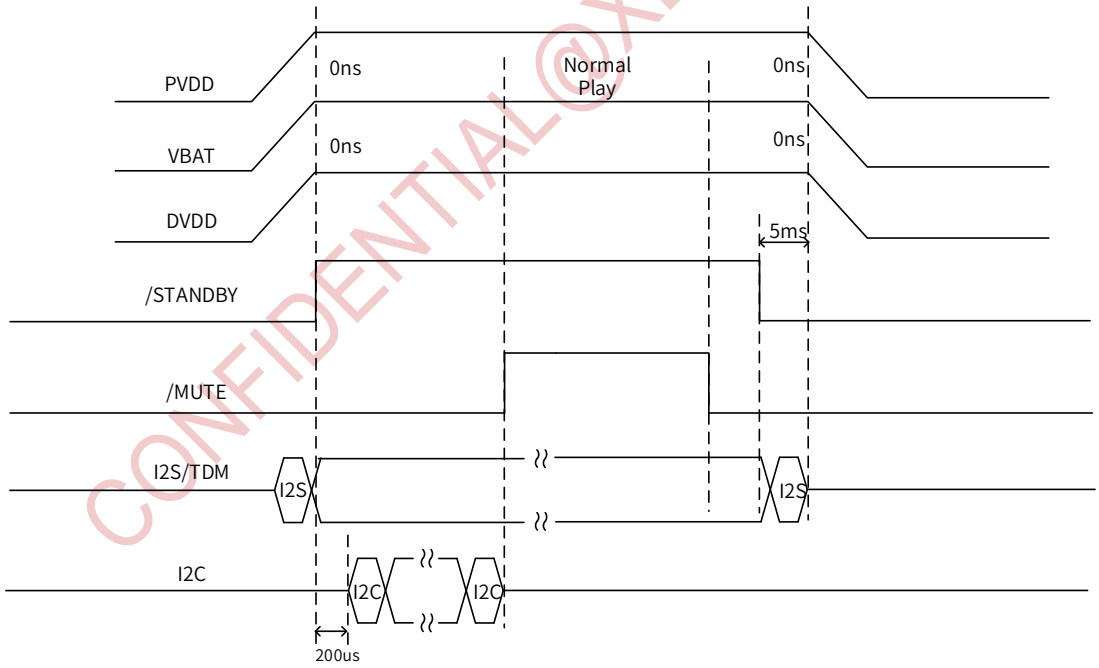
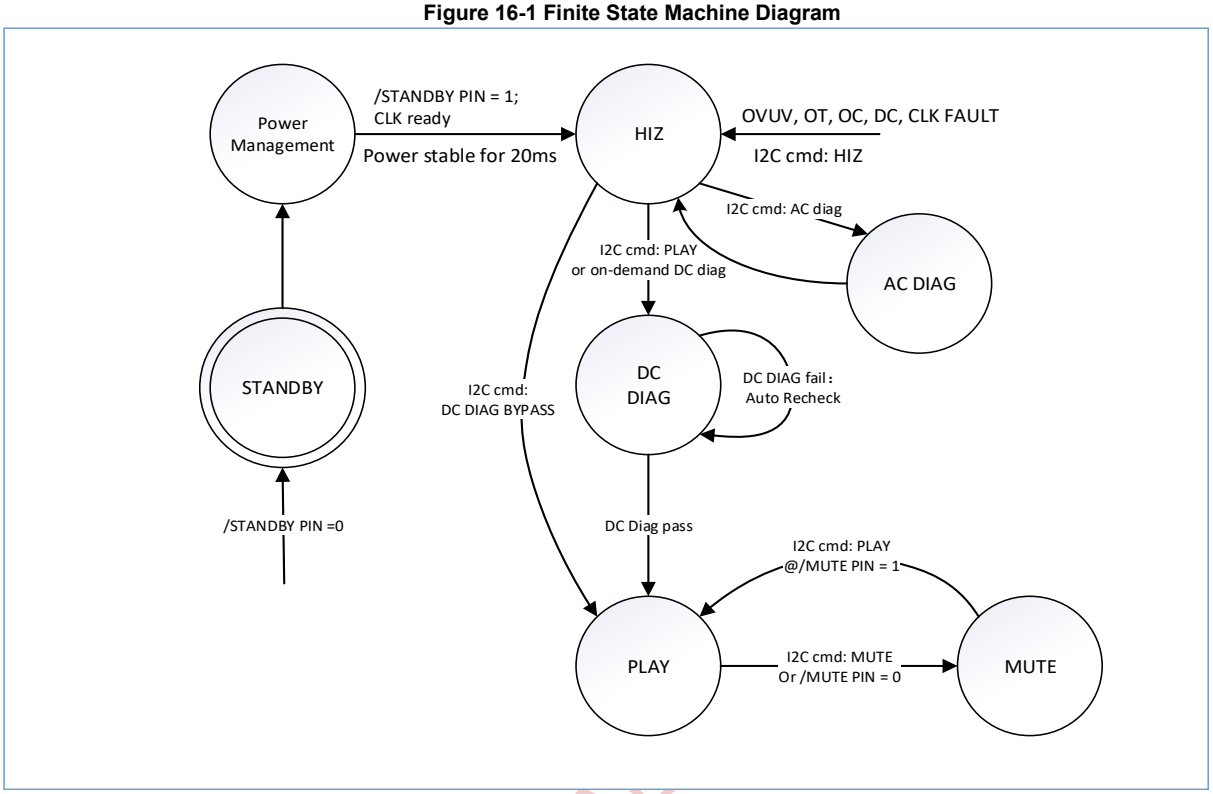


Figure 15-1 Power Up and Power Down Sequence

16. 有限状态机

CCD12076 的有限状态机由以下图表表示：

Figure 16-1 Finite State Machine Diagram



16.1 待机状态

当/STANDBY 引脚被拉低时，CCD12076 系统处于关闭状态，输出端保持接地偏置，所有寄存器将被复位，并且 I²C 通信不可用。

16.2 高阻态状态

当/STANDBY 引脚被拉高时，设备会自动进入高阻态（HIZ）。在这种状态下，I²C 通信仍然可用，输出处于高阻态。

16.3 直流诊断状态

CCD12076 系统在启动时默认运行直流诊断（DC diagnostic），以确保安全且无咔嗒声或爆音的启动。设备会在每次开始切换前运行直流诊断，以检测任何短路至电源、地、短路负载或开路负载的情况。如果存在这些异常情况，设备会重复运行诊断。直流诊断可以在所有通道并行运行时完成。在诊断状态下，I²C 通信仍然可用，输出保持在足够低的电平，以避免咔嗒声或爆音。

16.4 运行状态

当设备进入播放（PLAY）状态时，输出通道的 PWM（脉冲宽度调制）信号被激活。在这种状态下，音频信号处于开启状态，放大器完全正常工作。

16.5 静音状态

设备进入静音（MUTE）状态的方式有两种：通过将/MUTE 引脚拉低，或者通过 I²C 发送静音命令。在这种状态下，设备的 PWM 信号仍然保持激活，但音频信号被关闭。为了提供更好的听觉体验，设备在静音和取消静音过程中提供了平滑过渡功能，以避免在切换时出现咔嗒声或爆音。

17. 寄存器列表

Reg 0x00, default = 0x00				
Bit	Field	Type	Reset	Description
7	RESET_ I²C	RW	1'b0	0: Normal operation 1: Resets the device. Self-clearing, reads back 0.
6	MODE	RW	1'b0	0: BD mode 1：HE mode
5	PBTL_34	RW	1'b0	0: Channel 3 and 4 are in BTL mode 1: Channel 3 and 4 are in parallel BTL mode
4	PBTL_12	RW	1'b0	0: Channel 1 and 2 are in BTL mode 1: Channel 1 and 2 are in parallel BTL mode
3	CH1_LO_MODE	RW	1'b0	0: Channel 1 set normal/speaker mode 1: Channel 1 set line output mode
2	CH2_LO_MODE	RW	1'b0	0: Channel 2 set normal/speaker mode 1: Channel 2 set line output mode
1	CH3_LO_MODE	RW	1'b0	0: Channel 3 set normal/speaker mode 1: Channel3 set line output mode
0	CH4_LO_MODE	RW	1'b0	0: Channel 4 set normal/speaker mode 1: Channel 4 set line output mode

Reg 0x01, default = 0x32				
Bit	Field	Type	Reset	Description
7	HPF_BYPASS	RW	1'b0	0: High pass filter enabled 1: High pass filter disabled
6:5	OTW_CTRL	RW	2'd1	00: Global overtemperature warning set to 140°C 01: Global overtemperature warning set to 130°C 10: Global overtemperature warning set to 120°C 11: Global overtemperature warning set to 110°C
4	OC_CTRL	RW	1'b1	0: OCSD 1: 7.5A 1: OCSD 2: 10A
3:2	VOL_RATE	RW	2'd0	00: Volume update rate is 1 step / FSYNC 01: Volume update rate is 1 step / 2 FSYNCs 10: Volume update rate is 1 step / 4 FSYNCs 11: Volume update rate is 1 step / 8 FSYNCs
1:0	GAIN	RW	2'd2	00: Gain level 1 = 7.5 V peak output voltage 01: Gain Level 2 = 15 V peak output voltage 10: Gain Level 3 = 21 V peak output voltage 11: Gain Level 4 = 29 V peak output voltage

Reg 0x02, default = 0x60				
Bit	Field	Type	Reset	Description
7	RESERVED			
6:4	PWM_FREQ_SEL	RW	3'd6	000: 384 kHz, 001: 480 kHz (preferred) 010: 576 kHz 011: RESERVED 100: RESERVED 101: RESERVED 110: 2.11 MHz 111: RESERVED
3:0	RESERVED	RO	2'd0	No function

Reg 0x03, default = 0x04				
Bit	Field	Type	Reset	Description
7:6	INPUT_FS	RW	2'd0	00: 44.1 kHz 01: 48 kHz 10: 96 kHz 11: RESERVED
5	TDM_SLOT_SEL	RW	1'b0	0: First four TDM slots 1: Last four TDM slots
4	TDM_SLOT_SIZE	RW	1'b0	0: TDM slot size is 24-bit or 32-bit 1: NA
3	TDM_SLOT_SEL2	RW	1'b0	See TDM Mode for details. 0: Normal 1: Swapped
2:0	INPUT_FORMAT	RW	3'd4	000: 24- bit right justified 001: 20- bit right justified 010: 18- bit right justified 011: 16- bit right justified 100: I2S (16-bit or 24-bit) 101: Left justified (16-bit or 24-bit) 110: DSP mode (16-bit or 24-bit) 111: RESERVED

Reg 0x04, default = 0x55				
Bit	Field	Type	Reset	Description
7:6	STATECTL1	RW	2'd1	State control for channel 1 from I^2C 00: PLAY 01: Hi-Z 10: MUTE 11: DC load diagnostics
5:4	STATECTL2	RW	2'd1	State control for channel 2 from I^2C 00: PLAY 01: Hi-Z 10: MUTE 11: DC load diagnostics
3:2	STATECTL3	RW	2'd1	State control for channel 3 from I^2C 00: PLAY 01: Hi-Z 10: MUTE 11: DC load diagnostics
1:0	STATECTL4	RW	2'd1	State control for channel 4 from I^2C 00: PLAY 01: Hi-Z 10: MUTE 11: DC load diagnostics

Reg 0x05, Reg 0x06, Reg 0x07 and Reg 0x08, default = 0xCF				
Bit	Field	Type	Reset	Description
7:0	CH1-4_VOL	RW	8'd207	8-Bit Volume Control for each channel, register address for Ch1 is 0x05, Ch2 is 0x06, Ch3 is 0x07 and Ch4 is 0x08, 0.5 dB/step: 0xFF: 24 dB 0xCF: 0 dB 0 x07: –100 dB < 0x07: MUTE

Reg 0x09, default = 0x00				
Bit	Field	Type	Reset	Description
7	ABORT	RW	1'b0	0: Default state, clear after abort 1: Aborts the load diagnostics in progress
6:5	RESERVED	RW	2'd0	RESERVED
4	RESERVED	RW	1'b0	RESERVED
3	SLOL_DISCHARGE_BYP	RW	1'b0	0: Enable the waiting loop at the end of shorted / open load detection 1: Bypass the waiting loop at the end of shorted / open load detection
2	SLOL_BYP	RW	1'b0	0: Shorted load and open load detection are enabled 1: Shorted load, open load and line out detection are disabled
1	LDG_LO_EN	RW	1'b0	0: Line output diagnostics are disabled 1: Line output diagnostics are enabled
0	LDGBYP	RW	1'b0	0: Automatic diagnostics when leaving Hi-Z and after channel fault 1: Diagnostics are not run automatically

Reg 0x0A, default = 0x11				
Bit	Field	Type	Reset	Description
7:4	CH1_SL_THRESHOLD	RW	4'd1	DC load diagnostics shorted-load threshold 0000: 0.5 Ω 0001: 1 Ω 0010: 1.5 Ω ... 1001: 5 Ω
3:0	CH2_SL_THRESHOLD	RW	4'd1	DC load diagnostics shorted-load threshold 0000: 0.5 Ω 0001: 1 Ω 0010: 1.5 Ω ... 1001: 5 Ω

Reg 0x0B, default = 0x11				
Bit	Field	Type	Reset	Description
7:4	CH3_SL_THRESHOLD	RW	4'd1	DC load diagnostics shorted-load threshold 0000: 0.5 Ω 0001: 1 Ω 0010: 1.5 Ω ... 1001: 5 Ω
3:0	CH4_SL_THRESHOLD	RW	4'd1	DC load diagnostics shorted-load threshold 0000: 0.5 Ω 0001: 1 Ω 0010: 1.5 Ω ... 1001: 5 Ω

Reg 0x0C, default = 0x00				
Bit	Field	Type	Reset	Description
7	CH1_S2G	RO	1'b0	0: No short-to-GND detected 1: Short-To-GND Detected
6	CH1_S2P	RO	1'b0	0: No short-to-power detected 1: Short-to-power detected
5	CH1_OL	RO	1'b0	0: No open load detected 1: Open load detected
4	CH1_SL	RO	1'b0	0: No shorted load detected 1: Shorted load detected
3	CH2_S2G	RO	1'b0	0: No short-to-GND detected 1: Short-to-GND detected
2	CH2_S2P	RO	1'b0	0: No short-to-power detected 1: Short-to-power detected
1	CH2_OL	RO	1'b0	0: No open load detected 1: Open load detected
0	CH2_SL	RO	1'b0	0: No shorted load detected 1: Shorted load detected

Reg 0x0D, default = 0x00				
Bit	Field	Type	Reset	Description
7	CH3_S2G	RO	1'b0	0: No short-to-GND detected 1: Short-to-GND detected
6	CH3_S2P	RO	1'b0	0: No short-to-power detected 1: Short-to-power detected
5	CH3_OL	RO	1'b0	0: No open load detected 1: Open load detected
4	CH3_SL	RO	1'b0	0: No shorted load detected 1: Shorted load detected
3	CH4_S2G	RO	1'b0	0: No short-to-GND detected 1: Short-to-GND detected
2	CH4_S2P	RO	1'b0	0: No short-to-power detected 1: Short-to-power detected
1	CH4_OL	RO	1'b0	0: No open load detected 1: Open load detected
0	CH4_SL	RO	1'b0	0: No shorted load detected 1: Shorted load detected

Reg 0x0E, default = 0x00				
Bit	Field	Type	Reset	Description
7:4	RESERVED			
3	CH1_LO	RO	1'b0	0: No line output detected on channel 1 1: Line output detected on channel 1
2	CH2_LO	RO	1'b0	0: No line output detected on channel 2 1: Line output detected on channel 2
1	CH3_LO	RO	1'b0	0: No line output detected on channel 3 1: Line output detected on channel 3
0	CH4_LO	RO	1'b0	0: No line output detected on channel 4 1: Line output detected on channel 4

Reg 0x0F, default = 0x55				
Bit	Field	Type	Reset	Description
7:6	STATERPT1	RO	2'd1	00: PLAY 01: Hi-Z 10: MUTE 11: DC load diagnostics
5:4	STATERPT2	RO	2'd1	00: PLAY 01: Hi-Z 10: MUTE 11: DC load diagnostics
3:2	STATERPT3	RO	2'd1	00: PLAY 01: Hi-Z 10: MUTE 11: DC load diagnostics
1:0	STATERPT4	RO	2'd1	00: PLAY 01: Hi-Z 10: MUTE 11: DC load diagnostics

Reg 0x10, default = 0x00				
Bit	Field	Type	Reset	Description
7	CH1_OC	RO	1'b0	This status can be cleared by setting bit 7 at 0x21 register 0: No overcurrent fault detected 1: Overcurrent fault detected
6	CH2_OC	RO	1'b0	0: No overcurrent fault detected 1: Overcurrent fault detected
5	CH3_OC	RO	1'b0	0: No overcurrent fault detected 1: Overcurrent fault detected
4	CH4_OC	RO	1'b0	0: No overcurrent fault detected 1: Overcurrent fault detected
3	CH1_DC	RO	1'b0	0: No DC fault detected 1: DC fault detected
2	CH2_DC	RO	1'b0	0: No DC fault detected 1: DC fault detected
1	CH3_DC	RO	1'b0	0: No DC fault detected 1: DC fault detected
0	CH4_DC	RO	1'b0	0: No DC fault detected 1: DC fault detected

Reg 0x11, default = 0x00				
Bit	Field	Type	Reset	Description
7:5	RESERVED			
4	CLK_FAULT	RO	1'b0	This status can be cleared by setting bit 7 at 0x21 register 0: No clock fault detected 1: Clock fault detected
3	PVDD_OV	RO	1'b0	0: No PVDD overvoltage fault detected 1: PVDD overvoltage fault detected
2	VBAT_OV	RO	1'b0	0: No VBAT overvoltage fault detected 1: VBAT overvoltage fault detected
1	PVDD_UV	RO	1'b0	0: No PVDD undervoltage fault detected 1: PVDD undervoltage fault detected
0	VBAT_UV	RO	1'b0	0: No VBAT undervoltage fault detected 1: VBAT undervoltage fault detected

Reg 0x12, default = 0x00				
Bit	Field	Type	Reset	Description
7:5	RESERVED			
4	OTSD	RO	1'b0	This status can be cleared by setting bit 7 at 0x21 register 0: No global overtemperature shutdown 1: Global overtemperature shutdown
3	CH1_OTSD	RO	1'b0	This status can be cleared by setting bit 7 at 0x21 register 0: No overtemperature shutdown on Ch 1

				1: Overtemperature shutdown on Ch 1
2	CH2_OTSD	RO	1'b0	0: No overtemperature shutdown on Ch 2 1: Overtemperature shutdown on Ch 2
1	CH3_OTSD	RO	1'b0	0: No overtemperature shutdown on Ch 3 1: Overtemperature shutdown on Ch 3
0	CH4_OTSD	RO	1'b0	0: No overtemperature shutdown on Ch 4 1: Overtemperature shutdown on Ch 4

Reg 0x13, default = 0x20				
Bit	Field	Type	Reset	Description
7	RESERVED			
6	RESERVED			
5	POR	RO	1'b1	0: No DVDD POR has occurred 1 DVDD POR occurred
4	OTW	RO	1'b0	This status can be cleared by setting bit 7 at 0x21 register 0: No global overtemperature warning 1: Global overtemperature warning
3	OTW_CH1	RO	1'b0	This status can be cleared by setting bit 7 at 0x21 register 0: No overtemperature warning on channel 1 1: Overtemperature warning on channel 1
2	OTW_CH2	RO	1'b0	0: No overtemperature warning on channel 2 1: Overtemperature warning on channel 2
1	OTW_CH3	RO	1'b0	0: No overtemperature warning on channel 3 1: Overtemperature warning on channel 3
0	OTW_CH4	RO	1'b0	0: No overtemperature warning on channel 4 1: Overtemperature warning on channel 4

Reg 0x14, default = 0x00				
Bit	Field	Type	Reset	Description
7	MASK_OC	RW	1'b0	0: Report overcurrent faults on the FAULT pin 1: Do not report overcurrent faults on the FAULT Pin
6	MASK_OTSD	RW	1'b0	0: Report overtemperature faults on the FAULT pin 1: Do not report overtemperature faults on the FAULT pin
5	MASK_UV	RW	1'b0	0: Report undervoltage faults on the FAULT pin 1: Do not report undervoltage faults on the FAULT pin
4	MASK_OV	RW	1'b0	0: Report overvoltage faults on the FAULT pin 1: Do not report overvoltage faults on the FAULT pin
3	MASK_DC	RW	1'b0	0: Report DC faults on the FAULT pin 1: Do not report DC faults on the FAULT pin
2	RESERVED	RW	1'b0	RESERVED
1	MASK_CLIP	RW	1'b0	0: Report clipping on the WARN pin 1: Do not report clipping on the WARN pin
0	MASK_OTW	RW	1'b0	0: Report overtemperature warnings on the WARN pin 1: Do not report overtemperature warnings on the WARN pin

Reg 0x15, Reg 0x16 default = 0x00				
Bit	Field	Type	Reset	Description
7:0	RESERVED	RW	7'd0	No function

Reg 0x17, default = 0x10				
Bit	Field	Type	Reset	Description
7:4	REG_TDM_CH2_SEL	RW	4'd1	TDM Slot 0 to 7
3:0	REG_TDM_CH1_SEL	RW	4'd0	TDM Slot 0 to 7

Reg 0x18, default = 0x32				
Bit	Field	Type	Reset	Description
7:4	REG_TDM_CH4_SEL	RW	4'd3	TMD Slot 0 to 7
3:0	REG_TDM_CH3_SEL	RW	4'd2	TMD Slot 0 to 7

Reg 0x19, default = 0x00				
Bit	Field	Type	Reset	Description
7:0	REG_LTCMODE	RW	2'd0	00: Normal mode 1x: RESERVED 01: RESERVED

Reg 0x1F, default = 0x00				
Bit	Field	Type	Reset	Description
7:0	PVDD_METER	RO	7'd0	PVDD voltage=decimal code × 0.1256

Reg 0x20, default = 0x00				
Bit	Field	Type	Reset	Description
7:0	TEMPERATURE_METER	RO	7'd0	Temp in Celsius = 1.983 x decimal code - 272

Reg 0x21, default = 0x00				
Bit	Field	Type	Reset	Description
7	ANALOG_FAULT_CLEAR	WO	1'b0	Set this bit 1 to clear fault
6	PBTL_CH_SEL	RW	1'b0	0: PBTL normal signal source 1: PBTL flip signal source
5	RESERVED	RW	1'b0	RESERVED
4	RESERVED	RW	1'b0	RESERVED
3	OTSD_AUTO_REC_EN	RW	1'b0	0: OTSD is latched 1: OTSD is auto-recovery
2:1	RESERVED	RW	2'd0	RESERVED
0	RESERVED	RW	1'b0	RESERVED

Reg 0x22, default = 0x01				
Bit	Field	Type	Reset	Description
7:5	RESERVED			
4	CLIP_DUAL_EN	RW	1'b0	0: Report clip signal only at sine wave peak; 1: Report clip signal at both sine wave peak and valley
3	OT_WARN_UNLATCH	RW	1'b0	0: Latched OT to WARN PIN; 1: Unlatched OT to WARN PIN
2	CLIP_WARN_SEL	RW	1'b0	0: CH1-4 Clip Detect report to WARN pin 1: CH1-2 Clip Detect report to WARN pin, CH3-4 Clip Detect report to FAULT pin
1	CLIP_WARN_LATCH	RO	1'b0	0: Pin unlatch
0	CLIP_DETEC_EN	RW	1'b1	0: Clip detect disable 1: Clip detect enable

Reg 0x24, default = 0x00				
Bit	Field	Type	Reset	Description
7:4	RESERVED			
3	CLIP_CH4	RO	1'b0	This register will be set when clip detect occurred in corresponding channel, all the field can be cleared by writing bit 7 at register 0x21 0: No Clip Detect 1: CH4 Clip Detect
2	CLIP_CH3	RO	1'b0	0: No Clip Detect 1: CH3 Clip Detect
1	CLIP_CH2	RO	1'b0	0: No Clip Detect 1: CH2 Clip Detect
0	CLIP_CH1	RO	1'b0	0: No Clip Detect 1: CH1 Clip Detect

Reg 0x26, default = 0x00				
Bit	Field	Type	Reset	Description
7:5	RESERVED	RO	3'd0	No Function
4	RESERVED	RW	1'd0	RESERVED
2:0	HPF_CORNER	RW	3'd0	000: 3.7 Hz 001: 7.4 Hz 010: 15Hz 011: 30Hz 100: 59Hz 101: 118Hz 110: 235Hz 111: 463Hz

Reg 0x28, default = 0x0A				
Bit	Field	Type	Reset	Description
7:4	RESERVED			
3:0	GAIN_RAMP_CONTROL	RW	4'hA	[3] 1: Enable power up pop suppression; 0: Disable power up pop suppression [2] 1: Enable power down pop suppression 0: Disable power down pop suppression [1:0] Timer select: 00:30us/ step;01:60us/step;10:120us/step;11:240us/step

Reg 0x4C, default = 0x00				
Bit	Field	Type	Reset	Description
7:3	CLIP_LEVEL_SEL	RW	5'd0	00000: PVDD; 00001: PVDD* 1.03; 00010: PVDD*1.06; 00011: PVDD* 1.09: 00100:PVDD*1.122; 00101:PVDD*1.154; 00110:PVDD*1.188; 00111:PVDD*1.223; 01000:PVDD*1.259; ... 01111:PVDD*1.54; 10000:PVDD*0.63; 10001:PVDD*0.65; ... 11111:PVDD*0.97
2:0	RESERVED			

Reg 0x51, default = 0x00				
Bit	Field	Type	Reset	Description
7:4	RESERVED			
3:2	SS_MODULATION_DEPTH	RW	3'd0	Spread spectrum modulation depth

				00: 5%; 01: 2.5%; 10:7.5%,11:10%
1:0	RESERVED			

Reg 0x54, default = 0x00				
Bit	Field	Type	Reset	Description
7:6	RESERVED	RW		RESERVED
5:4	RESERVED	RW		RESERVED
3:0	REG SS HIGH LEVEL SPEED	RW	4'd0	SS high level controls ramp up and ramp down speed 0: High speed 1: Low speed others: Internal use

Reg 0x55, default = 0x10				
Bit	Field	Type	Reset	Description
7:0	SS_FREQ_SEL	RW	7'd17	0x11: SS frequency (FSW/16) 0x22: SS frequency / 2 0x33: SS frequency / 3 Others: Internal use

Reg 0x77, default = 0x00				
Bit	Field	Type	Reset	Description
7	SS - EN	RW	1'b0	1: Enable Spread Spectrum 0: Disable Spread Spectrum
6:0	RESERVED	RO		

18. 应用原理图

Figure 18-1 Typical 4-Channel BTL Application Schematic

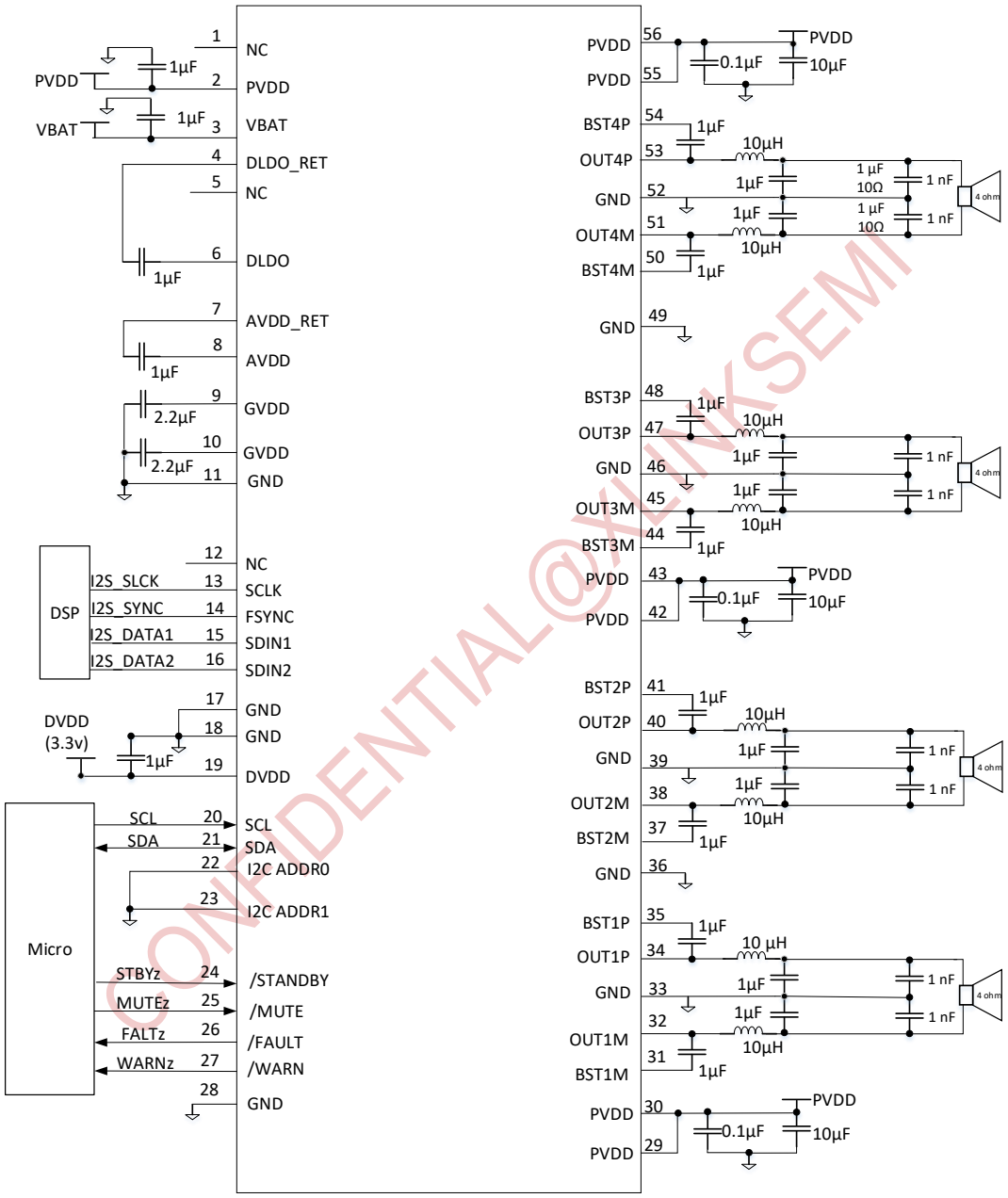
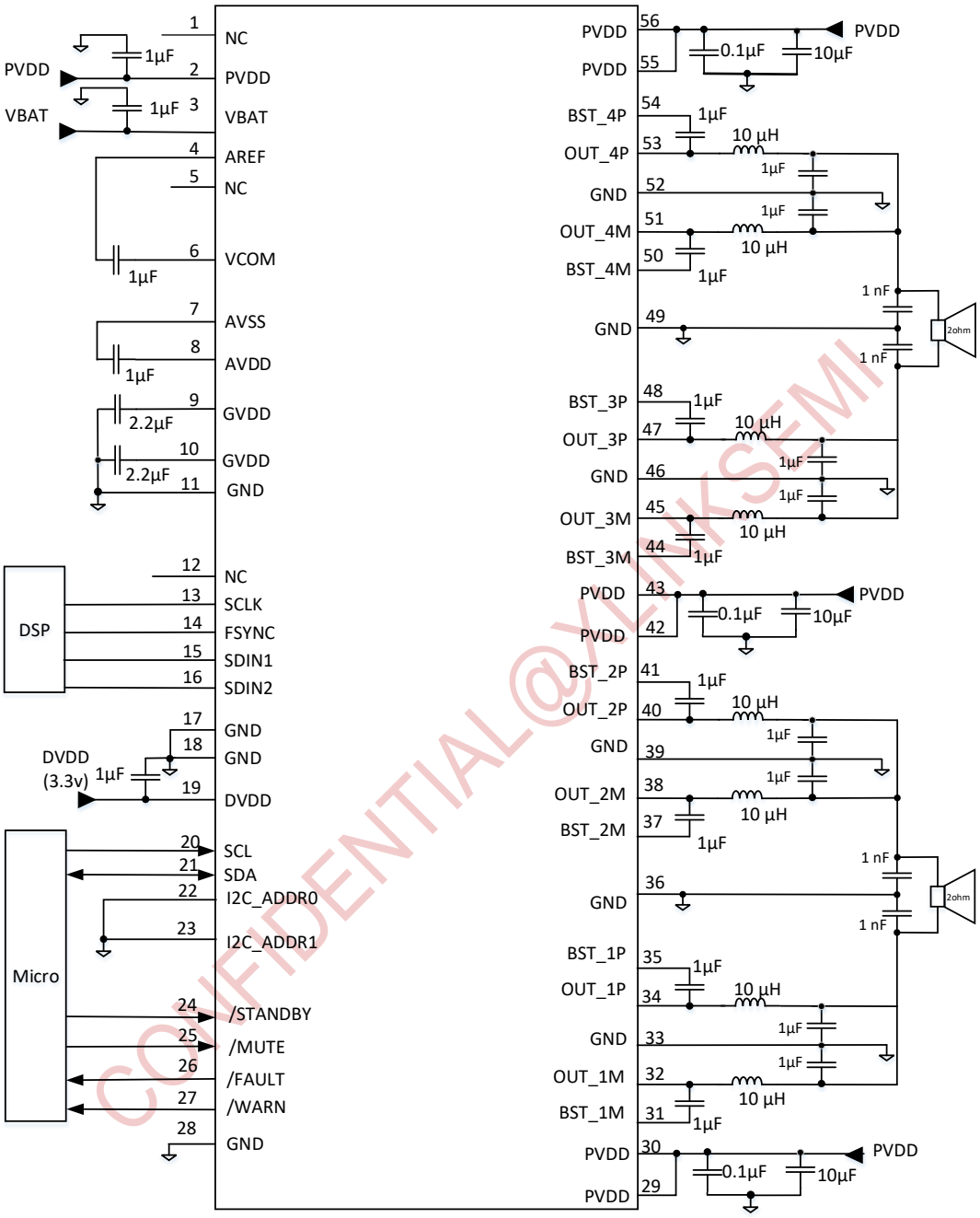


Figure 18-2 Typical 2-Channel PBTL Application Schematic



19. 封装信息

Figure 19-1 SSOP56-ep. Pad Up Package Outline

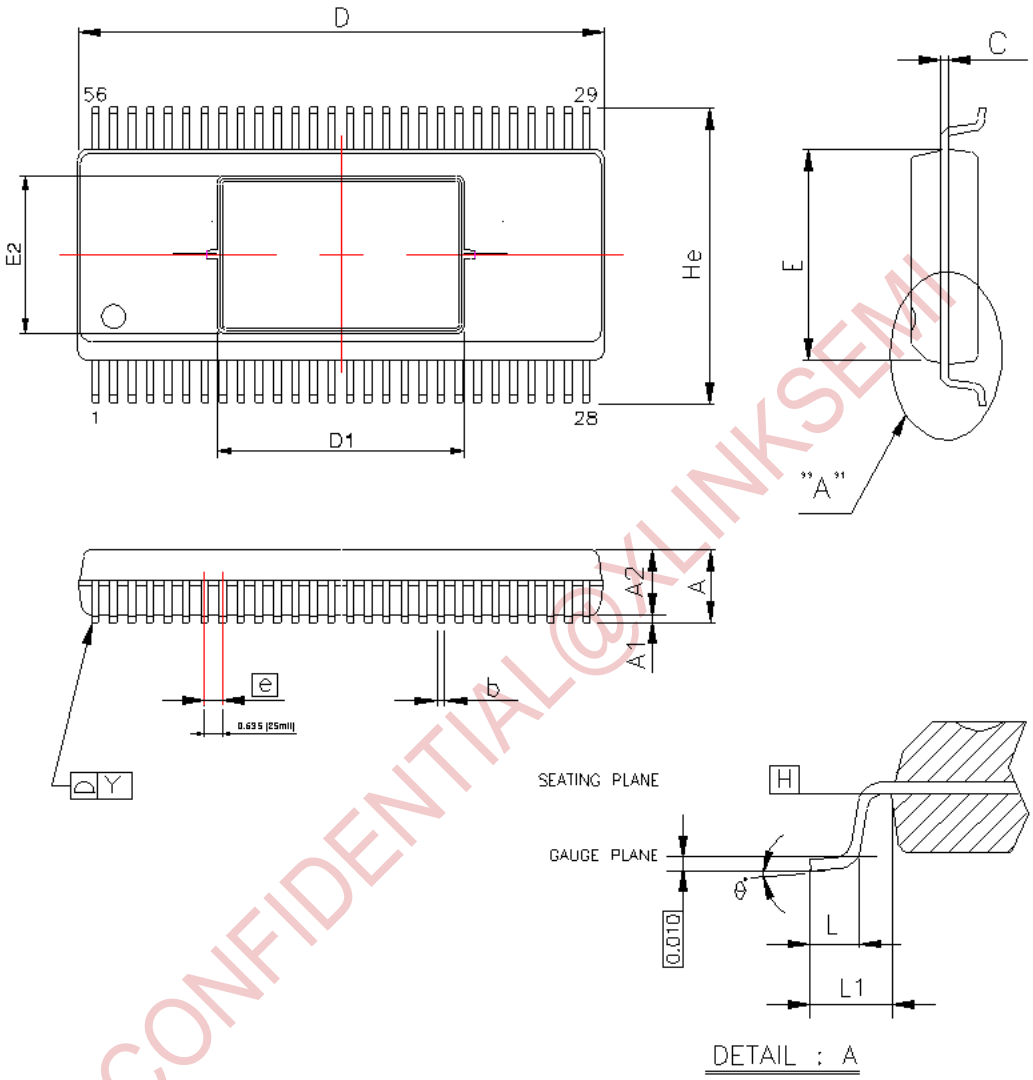


Table 19-1 SSOP56-ep. Pad Up Package Mechanical Data

Ref	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	2.450	2.580	2.710
A1	0.250		0.350
A2	2.200	2.280	2.360
b	0.203	0.254	0.330
c		0.203	
D	18.288	18.415	18.542
E	7.391	7.493	7.595
e		0.635	
He	10.033	10.312	10.668
L	0.508	0.762	1.016
L1		1.422	
Y			1.016
θ	0°		8°
D1		8.636	
E2		5.508	

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Datum plane H is located at the bottom of the mold parting line coincident with where the lead exits the body.
3. Dimensions E and D do not include mold protrusion. Allowable protrusion is 6mil per side. Dimensions E and D do include mold mismatch and are determined at datum plane H.
4. Dimension b does not include dam-bar protrusion.
5. The exposed thermal pad is designed to be attached to an external heat sink.

Figure 19-2 EXAMPLE BOARD LAYOUT

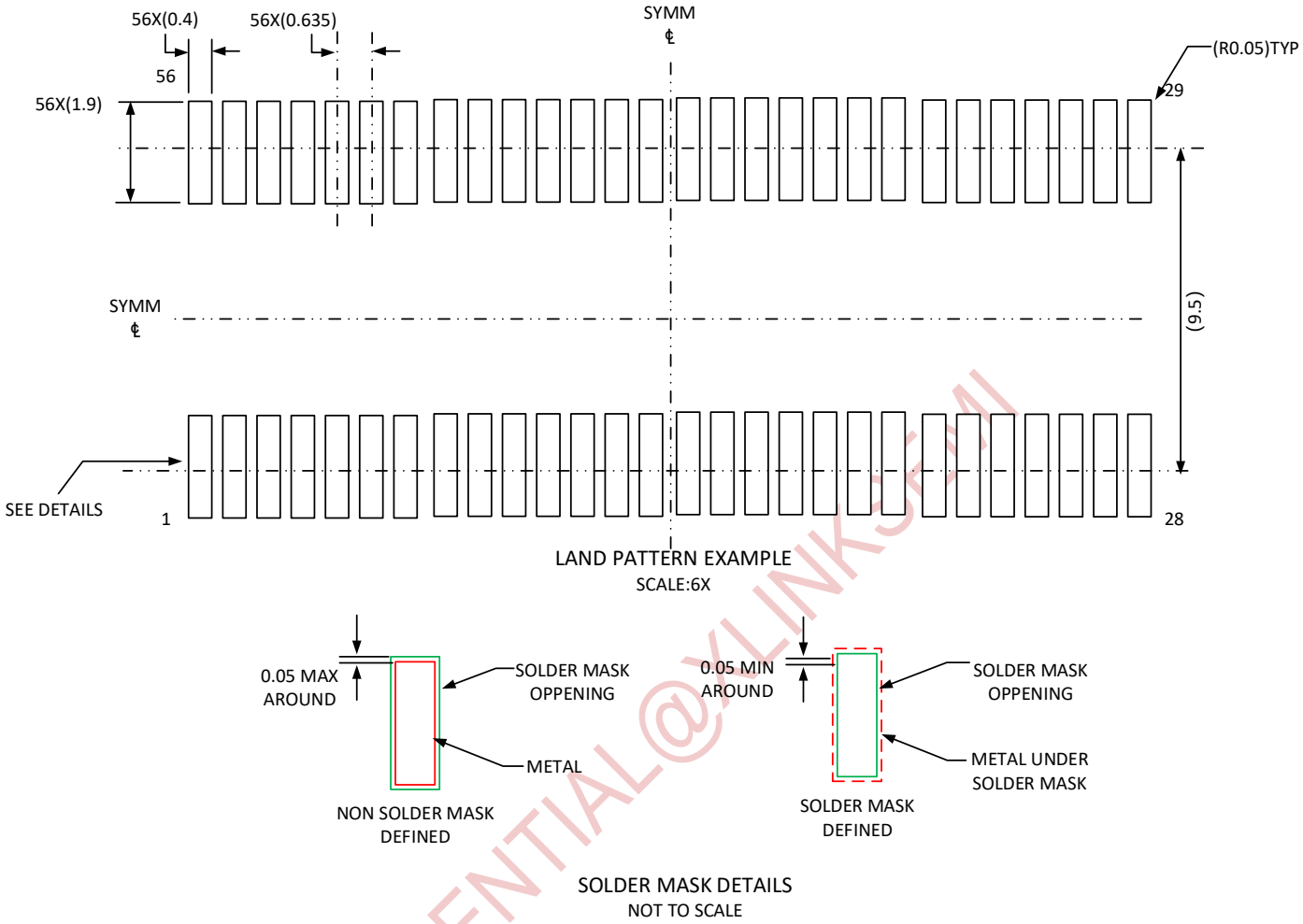
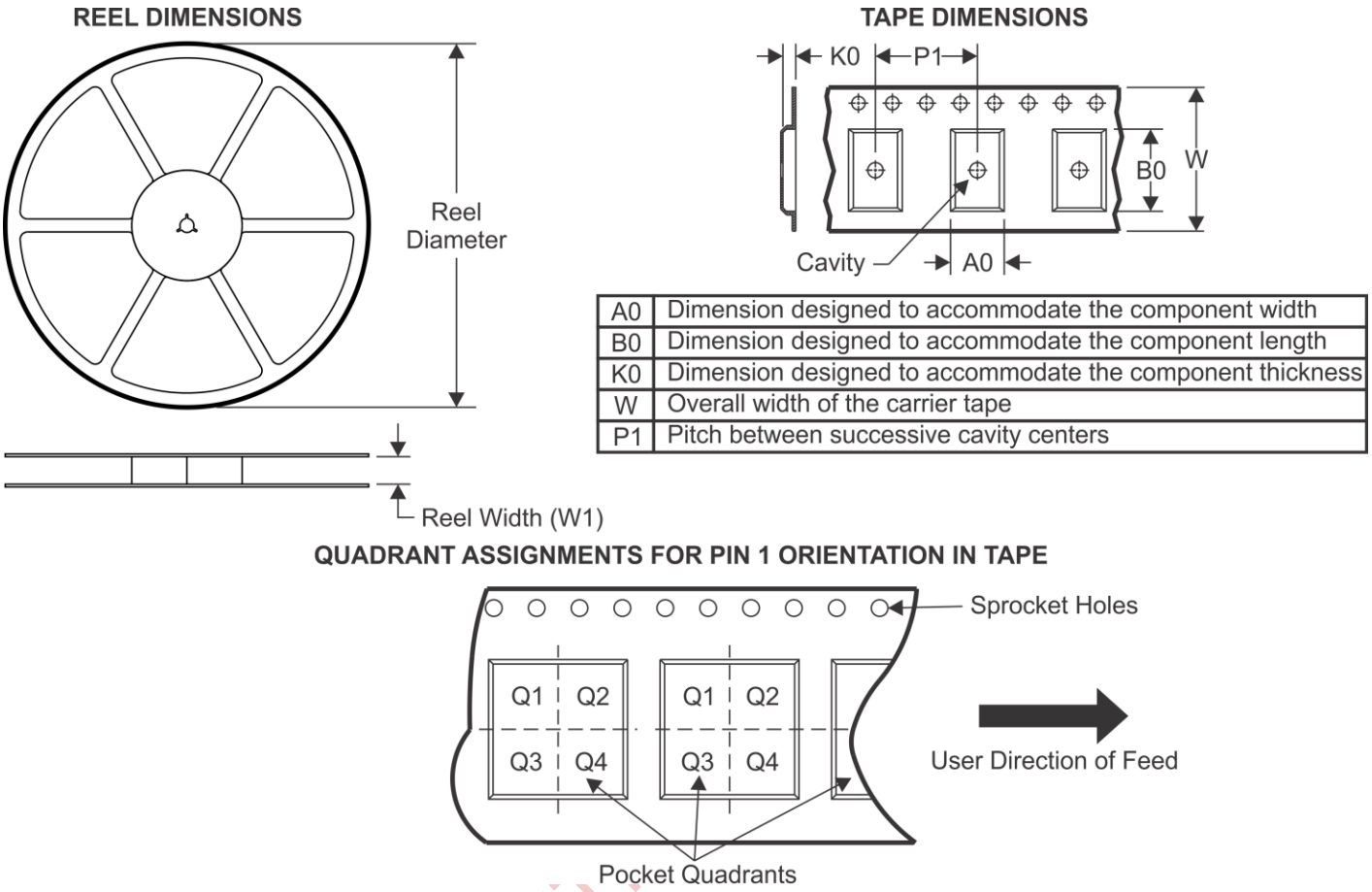


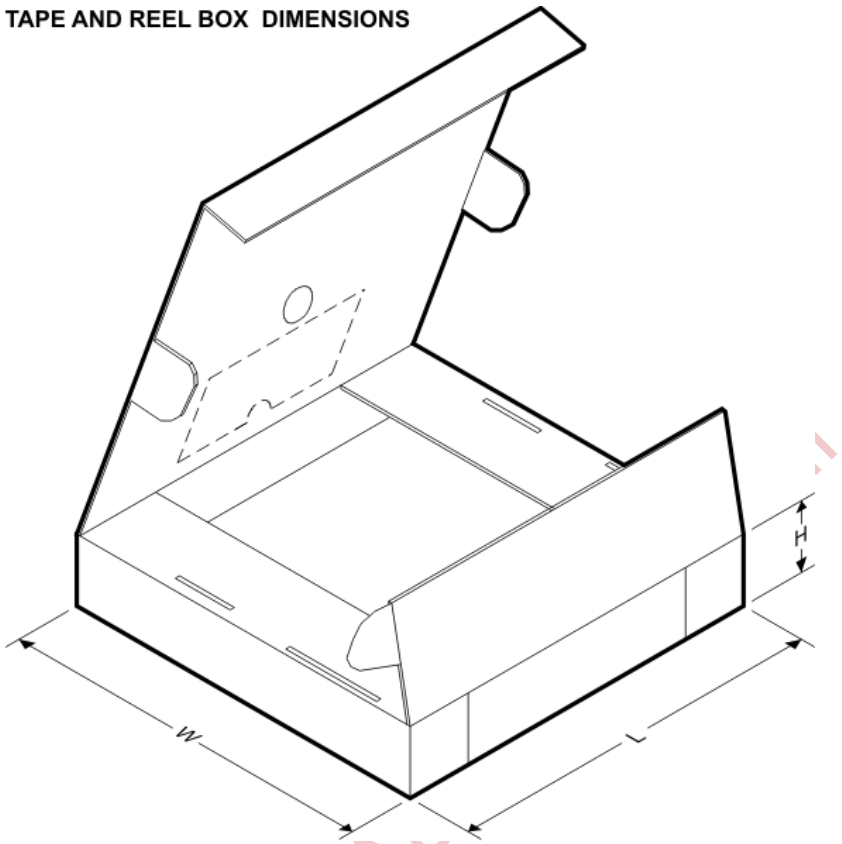
Figure 19-3 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

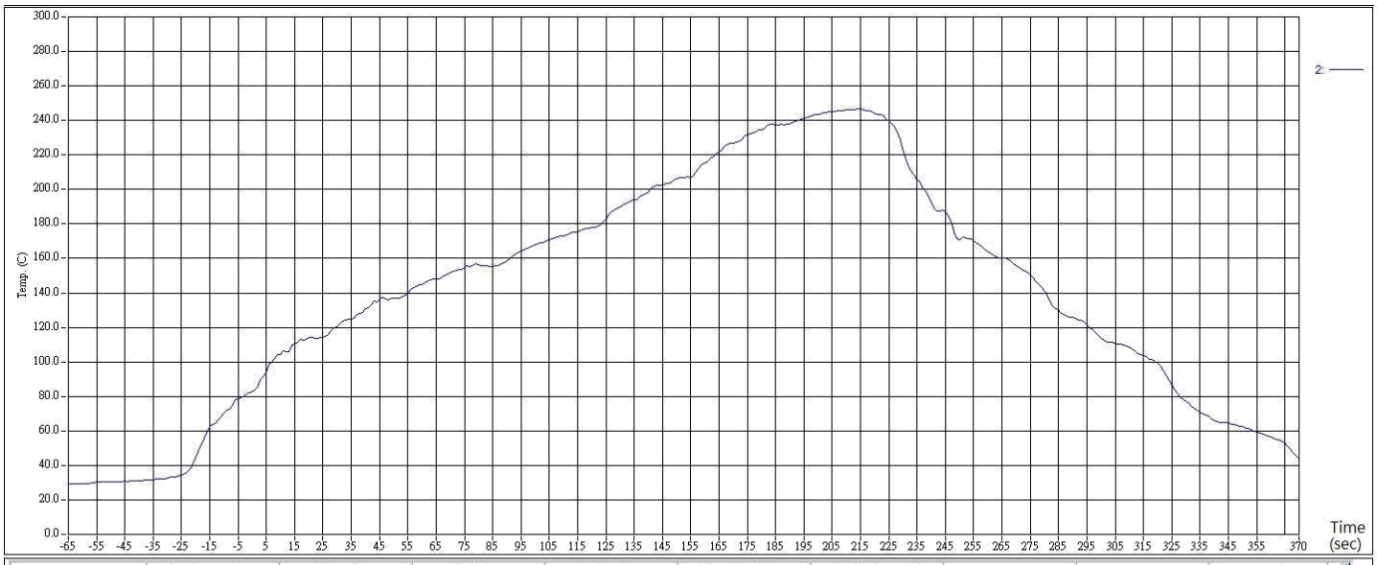
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CCD12076	SSOP	56	1000	330.0	32.4	10.97	18.84	3.5	16.0	32.0	Q1

Figure19-4 Tape and Reel Box Dimensions



Device	Package Type	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CCD12076	SSOP	56	1000	356.0	338.0	51.1

20. 焊接信息



	Ave Ramp up rate(T)	Holding Time	Peak Temp.	Liquidus Temp.	Time Above Temp.	Ave Cooling rate(T)			Result
Boundary	217.00-245.00 C	150.00-200.00 C	-------	217.00 C	240.00 C	245.00-217.00 C			
Range	0.00-3.00 (C/sec)	60.00-120.00 (sec)	245.00-250.00 (C)	60.00-150.00 (sec)	30.00-40.00 (sec)	6.00-0.00 (C/sec)			
sensor2	0.64	72.00	246.62	70.00	32.00	2.51			Ok

21. 修订历史

Table 21-1 文档修订历史

Date	Revision	Changes
2024/12/18	V1.0	Initial release
2025/5/23	V1.1	Update audio output data, reg 0x1F,0x20
2025/7/10	V1.2	Update Table12-1，reg 00,54, 55

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